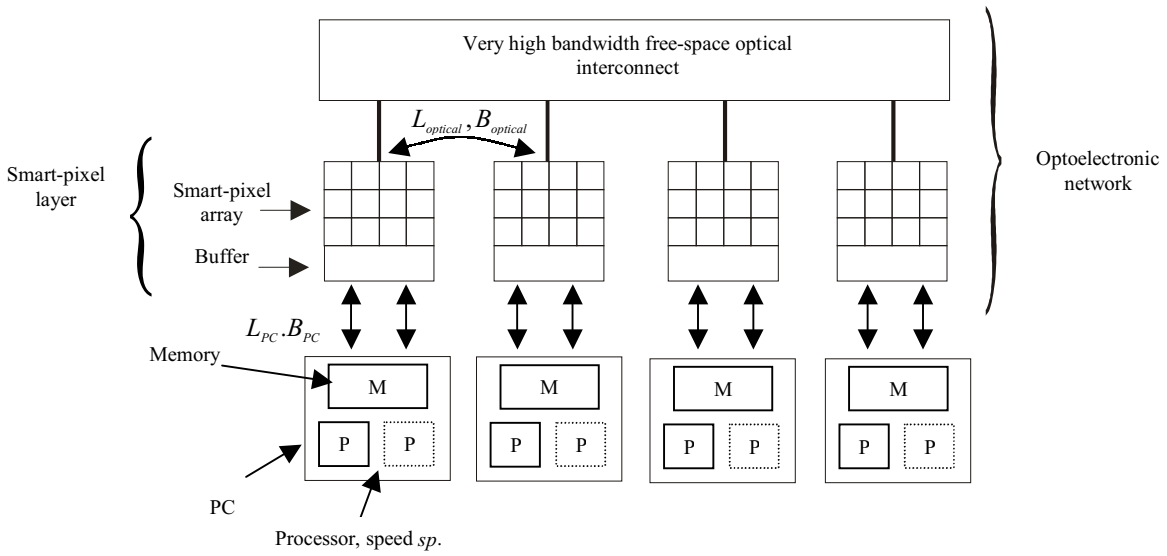
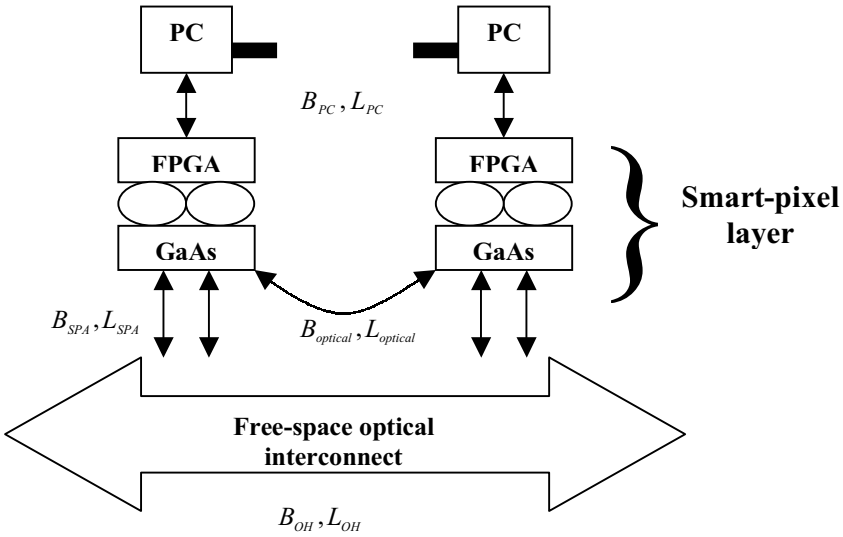
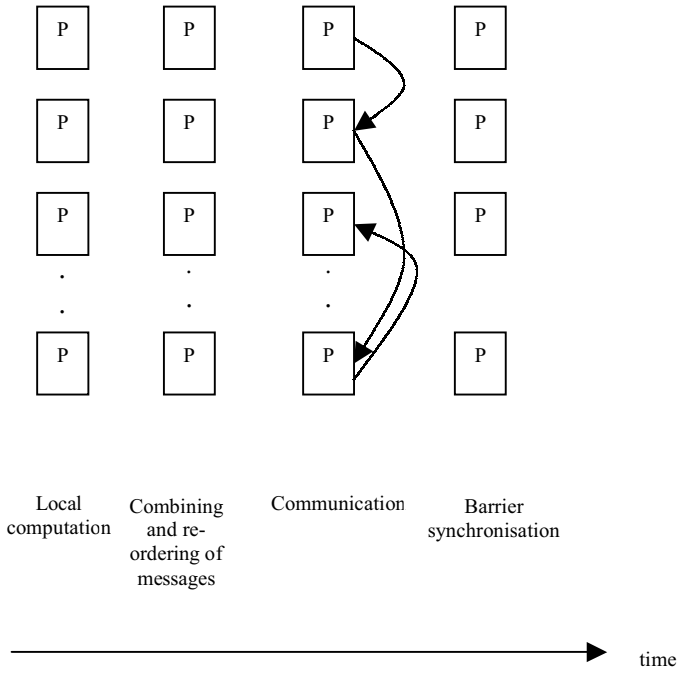
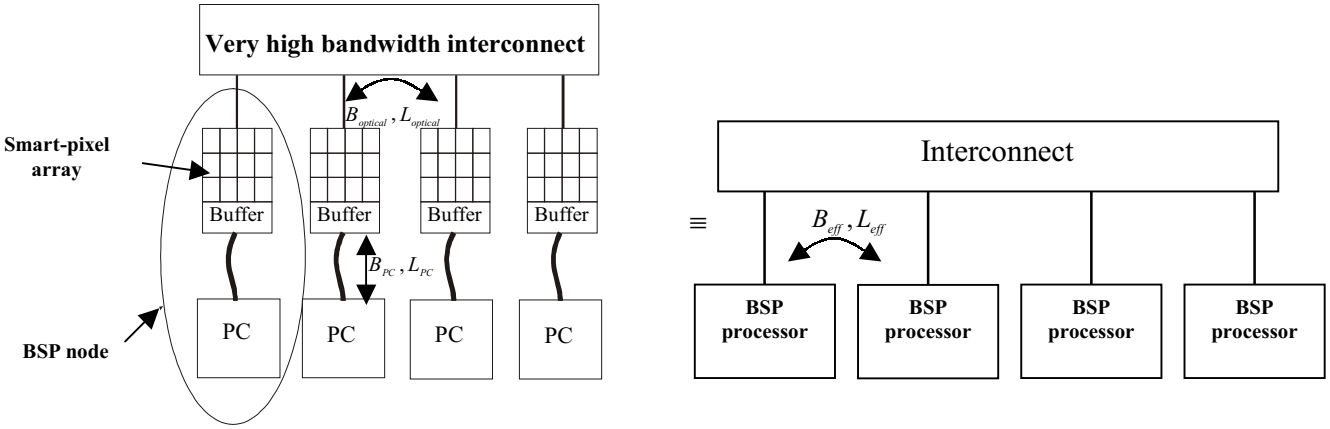
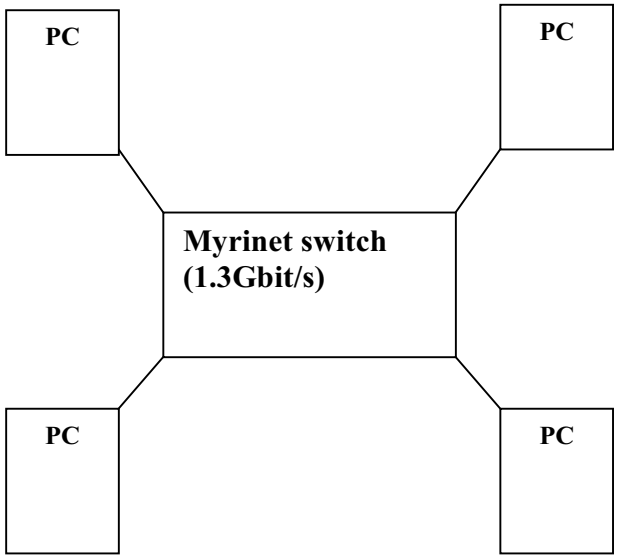
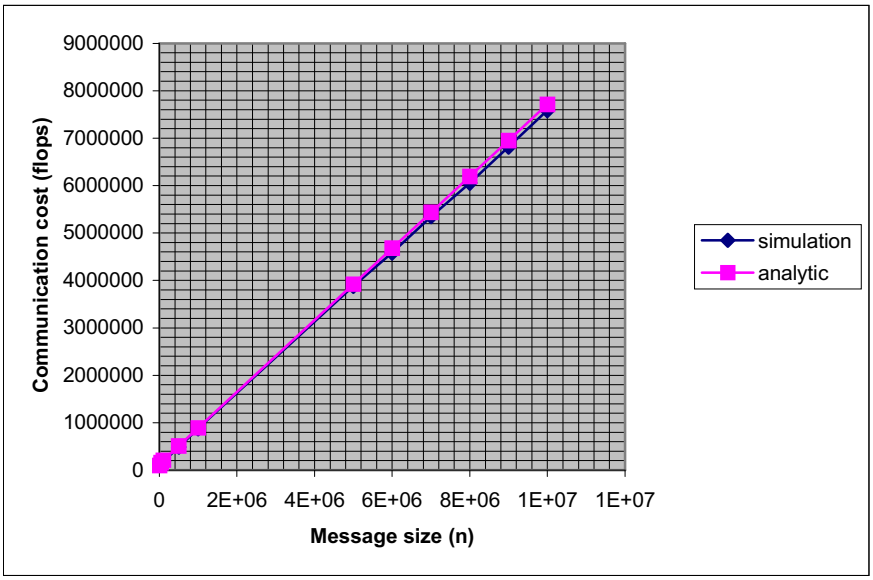

Very high bandwidth free-space optical interconnect
$L_{optical}, B_{optical}$
Smart-pixel layer
Smart-pixel array
Buffer
Optoelectronic network
L_{PC}, B_{PC}
Memory
M
P
P
PC
Processor, speed *sp*.

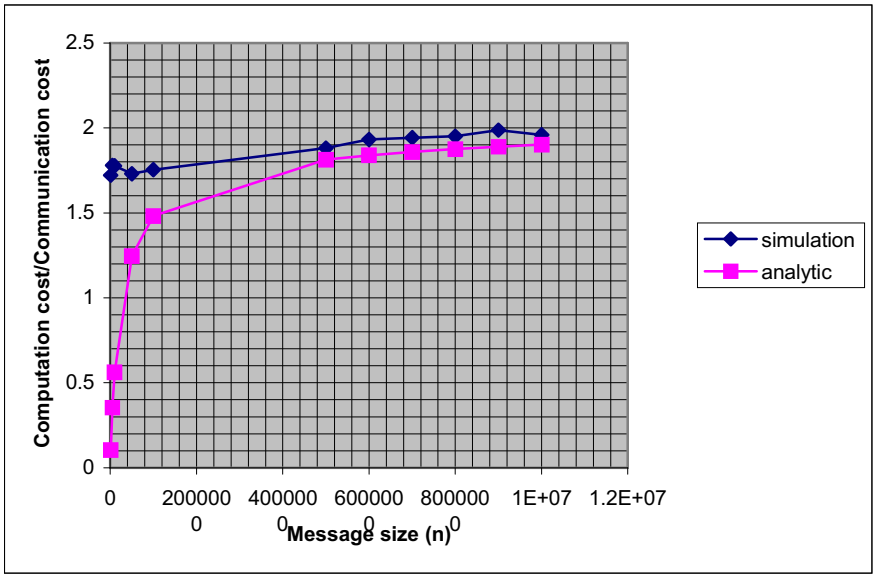

PC
PC
B_{PC}, L_{PC}
FPGA
FPGA
Smart-pixel layer
GaAs
GaAs
B_{SPA}, L_{SPA}
$B_{optical}, L_{optical}$
Free-space optical interconnect
B_{OH}, L_{OH}

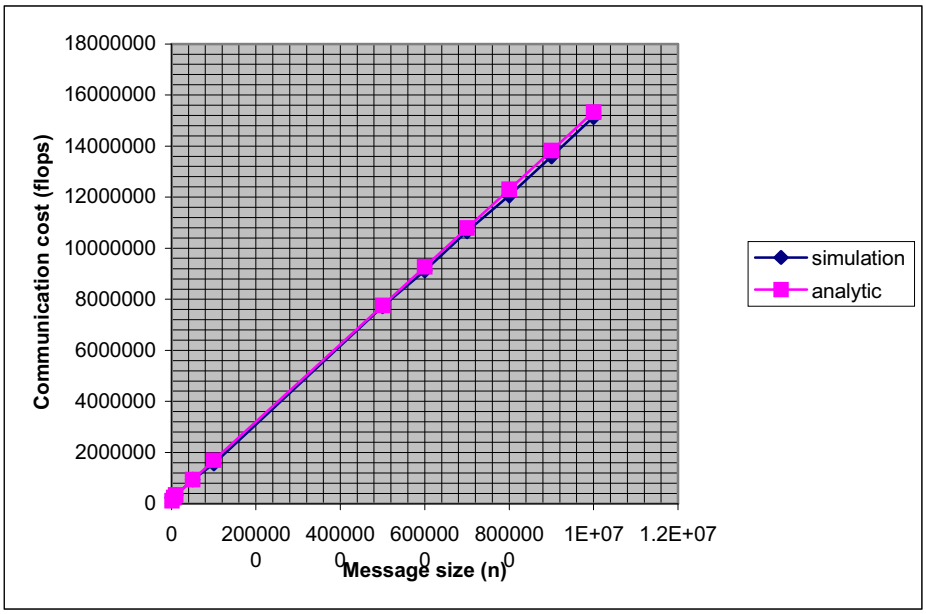

P
Local computation
Combining and re-ordering of messages
Communication
Barrier synchronisation
time


Very high bandwidth interconnect
$B_{optical}, L_{optical}$
Smart-pixel array
Buffer
Buffer
Buffer
Buffer
B_{PC}, L_{PC}
BSP node
PC
PC
PC
PC
≡
Interconnect
B_{eff}, L_{eff}
BSP processor
BSP processor
BSP processor
BSP processor


PC
PC
Myrinet switch
(1.3Gbit/s)
PC
PC


9000000
8000000
7000000
6000000
5000000
4000000
3000000
2000000
1000000
0
Communication cost (flops)
0
2E+06
4E+06
6E+06
8E+06
1E+07
1E+07
Message size (n)
simulation
analytic


2.5
2
1.5
1
0.5
0
Computation cost/Communication cost
0
200000
400000
600000
800000
1E+07
1.2E+07
Message size (n)
simulation
analytic


18000000
16000000
14000000
12000000
10000000
8000000
6000000
4000000
2000000
0
Communication cost (flops)
0
200000
400000
600000
800000
1E+07
1.2E+07
Message size (n)
simulation
analytic

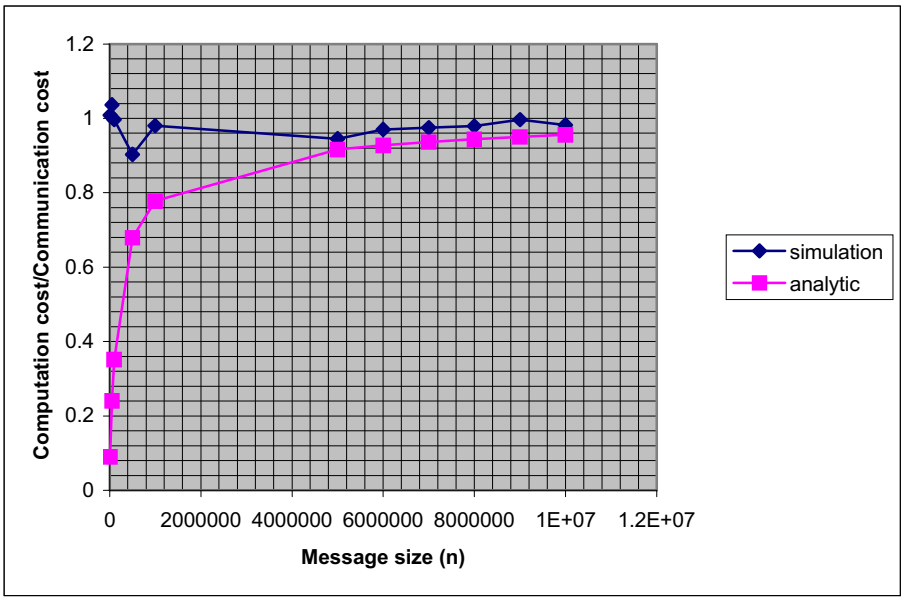

1.2
1
0.8
0.6
0.4
0.2
0
Computation cost/Communication cost
0
2000000
4000000
6000000
8000000
1E+07
1.2E+07
Message size (n)
simulation
analytic

Figure 1: The proposed optoelectronic architecture based on the concept of a computational cluster, with a high speed optical interconnect. The smart-pixel layer is used as an interface between the computational layer and the interconnect, with the intention of overcoming the problems presented by the bandwidth bottleneck in the links from/to the PCs. The processors in dotted boxes indicate the possibility of using dual processor PCs.

Figure 2: Characterisation of inter-smart-pixel array communication. Communication between a smart-pixel array and the optical interconnect is characterised by B_{SPA} and L_{SPA} . The available bandwidth of the optical interconnect is B_{OH} and the optical time-of-flight is L_{OH} . The effective bandwidth and latency in communication between a pair of smart-pixel arrays are $B_{optical}$ and $L_{optical}$ respectively.

Figure 3: Schematic depiction of a BSP computation. Each processor performs a local computation, and this is followed by a communication phase (after combining and re-ordering of data). A barrier synchronisation is then implemented across all the processors.

Figure 4: Implementation of the BSP model on the optoelectronic architecture. A BSP processor consists of a PC and its corresponding smart-pixel array and buffer. Communication between PCs and the smart-pixel layer is allowed during local computation but inter-BSP processor communication is not. Equivalence with two-layered system is indicated.

Figure 5: Schematic of a PC cluster with Myrinet switch.

Figure 6: The communication cost and the ratio of computation cost to communication cost as a function of *n*, for word size of 16 bits.

Figure 7: The communication cost and the ratio of computation cost to communication cost as a function of *n*, for word size of 32 bits.