An Optoelectronic Neural Network Scheduler Implementation and Operation

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Abstract

The design of the next-generation of the optoelectronic scheduler for a packet switch is outlined. The new demonstrator system is faster and more compact than the previous design as well as having greater operational flexibility. The use of off-the-shelf Digital Signal Processors to provide the neural thresholding functions allows the functionality of the network to be altered and new applications to be tackled with minimal alteration to the optoelectronic hardware. The DSPs, which are combined with Analogue-to-Digital and Digital-to-Analogue converters to create an 8-bit hybrid analogue/digital electronic subsystem, are operated in a time-multiplexed manner enabling each of the four DSPs to handle 16 input and 16 output channels. The electronic subsystem is combined with a Si photodetector array and an array of Vertical Cavity Surface-Emitting Lasers (VCSELs) to form the complete demonstrator. The optical components have been mounted on an optomechanically designed baseplate. This packaging scheme facilitates focus adjustments and mechanical and thermal stability for VCSELs whose total power consumption is estimated to be 10W. The entire optomechanical package will hold all the optical components within a miniature space of approximately 12cm x 15cm x 20cm.

The role of diffractive optical elements to provide the fixed weight interconnections between the neurons in the system is analysed. This analysis allows the limitations on the size of network which can be implemented using current DOE fabrication techniques to be derived and strategies for the increase of these limits to be studied.

The key to utilising the parallelism of a neural network is matching the network topology to the problem as closely as possible. The choice of DOE element and the flexibility given by the programmability of the DSPs allows us to achieve this for a number of interesting problems, e.g. Travelling Salesman (and related optimisation), feature extraction and process control. We have mapped examples of these problems and validated the mappings using a highly accurate simulator of the physical network. Experimental results will be used to verify the theoretical predictions made by simulation.
Vertical Cavity Surface-Emitting Laser Array and Driver Circuits

- The optical output from each neuron, which drives the inhibitory interconnections between the neurons, is supplied by a VCSEL array.

![VCSEL Image]

- Mean Threshold Current $I_{th} = 2.57 \pm 0.05 \text{mA}$
- Mean Threshold Voltage $V_{th} = 1.95 \pm 0.01 \text{V}$
- VCSEL Resistance $R_{VCSEL} = A \times V^B$ where $A = 6.7867, B = -0.7941$
- Operating Wavelength $\lambda = 960 \pm 0.25 \text{nm}$

- VCSEL beam shape is Gaussian with an 8° divergence. After projection through the optical elements, the average beam diameter is 64.7 μm compared to a diffraction limited spot size for the optical system of 34 μm.

![Beam Intensity Graph]

VCSEL Driver Circuits are required to supply current to switch the VCSELs on with sufficient optical power to produce a measurable voltage swing at the photodetector array. The optical power incident upon the detector array is equal to,

$$P_{\text{detector}} = \frac{P_{\text{output}} \cdot \text{efficiency}}{4(N-1)}$$

which for the optical system used in the demonstrator produces $0.07 \times P_{\text{output}}$ at the detector.

Two different driver circuits are used in the demonstrator, the first a digital circuit based around a standard octal driver (Texas Instruments SN74HC573AN) and the second a semi-custom ASIC analogue driver.

**Digital Driver**

![Digital Driver Diagram]

The resistors used in the digital driver were $R_1 = 470 \Omega$ and $R_2 = 100 \Omega$ supplying a high current to the VCSEL of 7.1 mA for an input voltage of 5V. The LE (Latch Enable) pin of the octal drive chip allows the VCSEL output to be selectively decoupled from the voltage input. The simulated output from the analogue driver, which has been fabricated using a 2-poly 2-metal CMOS process, is shown below.

![Analogue Driver Graph]

The digital driver has been used to test the operation of the VCSEL array in both modulated and steady-state modes.

- $P_{\text{average}} = 1.07 \text{mW} \text{ with No Modulation}$
- $P_{\text{average}} = 0.90 \text{mW} \text{ with 3kHz Modulation}$

**VCSEL Output Power for one row of 8x8 array**

![VCSEL Output Power Graph]

**Detected signal for 5kHz VCSEL modulation**

![Detected Signal Graph]
Neural Network Switch Controller: System Overview

The Hopfield neural network is composed of an array of thresholding processing elements, called neurons, and inhibitory interconnections between those neurons. The dynamic behaviour of the network is governed by,

\[ \frac{d x_{ab}}{dt} = I_{ab} - \lambda x_{ab} - \sum_{i \neq a} \sum_{j \neq b} W_{iabj} y_{ij} + t_{ab} \]

\[ y_{ij} = o_{\text{max}} + \frac{o_{\text{max}} - o_{\text{min}}}{1 + \exp(\beta x_{ij})} \]

The optoelectronic neural network uses optical interconnections to implement the \( W_{iabj} \). The neuron processing is performed by dedicated electronics.

Electronic System

Optical System

The specific inhibitory interconnection pattern used in this demonstrator is given by,

\[ W_{iabj} = \eta, \text{ if } i = a \text{ or } j = b, \]
\[ W_{iabj} = 0, \text{ if } i = a \text{ and } j = b, \]
\[ W_{iabj} = 0, \text{ otherwise} \]

Reference

Diffractive Optical Element Design and Fabrication

The inhibition pattern required by the Hopfield network is implemented by a space-invariant scalar-domain far-field diffractive optical element. This DOE was designed using a combination of a pixellated iterative Fourier transform algorithm and a trapezoidal closed-form optimisation technique. This design procedure produces DOEs which have high efficiency (> 60%) and low non-uniformity (< 0.5%).

The total intensity in the \((m,n)\)th diffraction order of a phase grating constructed from \(R\) rows of \(\pi R\) trapezoids per row is,

\[
F_{mn} = \frac{i}{2\pi R} \sum_{r=1}^{R} \sum_{j=1}^{\pi R} \left( \frac{\sin(\pi m d_{jr} - \phi_{jr})}{\pi m d_{jr}} \right) \left( \frac{\sin(\pi n d_{jr})}{\pi n} \right)
\]

\[
F_{mn} = \frac{i}{2\pi R} \sum_{r=1}^{R} \sum_{j=1}^{\pi R} \left( \frac{\sin(\pi m a_{jr} + \phi_{jr})}{\pi m a_{jr}} \right) \left( \frac{\sin(\pi n a_{jr})}{\pi n} \right)
\]

where

\[
\alpha = -i(\phi_{jr} + \pi(\phi_{j} + \phi_{jr})) + \pi(\phi_{jr} - 1)
\]

\[
\beta = -i(\phi_{jr} + \pi(\phi_{j} + \phi_{jr})) - \pi(\phi_{jr} - 1)
\]

The overall efficiency \((\eta)\) of the DOE is measured by summing the \(F_{mn}\) over the set of "on" diffraction orders \((M)\). The non-uniformity or reconstruction error of the DOE is a measure of the deviation of the DOE output from the desired output. It is defined as,

\[
\Delta \eta = \max_{m,n} \frac{N(M) F_{mn}}{\eta}
\]

The DOE design is fabricated using standard photolithography and reactive ion etching. Gratings with minimum feature sizes down to 2\(\mu\)m have been produced using the in-house fabrication facilities at Heriot-Watt.

Fabrication errors increase the reconstruction error of the fabricated DOE and arise from a number of different sources.

- Photolithographic rounding errors and feature elimination as shown below.
- Layer misalignment for multilevel phase profiles.
- Etch depth inaccuracy.
- Etch non-uniformity across the element.

The dominant fabrication errors are the photolithographic rounding errors and the layer misalignment. Etch depth inaccuracies are typically less than 1% and etch non-uniformity across the element can be ignored for the scalar domain elements under consideration here. The cumulative reconstruction degradation is of the order of 1 - 2% per etching step, i.e. a 16 phase-level DOE will have a total non-uniformity of between 4% and 8% after fabrication.

See Also: Invited Paper 3, M.R. Taghizadeh (Wednesday 13.00, Panorama Room.)

Crossbar Optimisation Diffractive Optical Element.

The DOE required to implement the inhibitory interconnection for an 8\(\times\)8 Hopfield network is shown below.

The period of the DOE is determined by the optical system the element will be used in. The optical system of the demonstrator has the following parameters.

- Effective focal length of lens, \(f = 150\)mm
- Operating wavelength, \(\lambda = 960\)nm
- Required diffraction order separation, \(s = 1.5\)mm

The DOE period is given by,

\[
T = \frac{n \lambda}{s}
\]

\(n\) is the number of orders between adjacent "on" diffraction orders and this produces a DOE period of 94nm for the optical system used in the demonstrator. The minimum feature size of the final design is 1.8\(\mu\)m and the measured efficiency is 0.5.

The small minimum feature size of the basic interconnection DOE inhibits the accurate fabrication of the element. By using every second diffraction order rather than every order, the period and hence the minimum feature size of the grating can be increased. The period of the double order spacing grating, which is the one used in the demonstrator hardware, is 18\(\mu\)m with a minimum feature size of 3.6\(\mu\)m.

The larger minimum feature size produces a significant improvement in the reconstruction error of the fabricated grating.
Neural Demonstrator System

VCSEL Array and Driver

Digital Signal Processor Boards

Detector Array

Optomechanical Baseplate and Optical Subsystem

20cm
Network Simulation and Scalability Studies.

The performance of all the subsystems of the network demonstrator have been characterised and the response functions used to implement a number of simulation codes which enable the behaviour of the whole network to be studied. The network operation has been studied from both an electronic and optical viewpoint and a measure of the scalability of the architecture has been derived.

The digitally driven network displays superior convergence speed at the expense of a marginal decrease in optimisation efficiency.

The performance of the network in the presence of optical ‘noise’ generated by the nonuniformity of the diffractive optical element has been studied.

The network is assumed to be operating correctly when > 90% of the test runs produce N “on” neurons for an N x N network. The reconstruction error at which this criterion is no longer satisfied is defined as the maximum allowable reconstruction error. For the 8 x 8 network demonstrator this value is 4%.

The maximum allowable reconstruction error for a network of size N x N is given by,

\[
\Delta \sigma_{\text{max}} = \frac{1}{AN + B}
\]

with \( A = 3.398 \) and \( B = -1.435 \). Assuming a minimum fabrication reconstruction error of 1% per mask level, the diffractive optical element used to provide the inhibitory interconnection between the neurons must be binary and the maximum size of network which can be implemented using the available free-space optical interconnection technologies is 30 x 30.

The average delay in network cycles (the length of time between new requests arriving at the network) is shown to rise with increasing network load.
Silicon Photodetector Array and Amplifier
An off-the-shelf Si photodetector array (Centronic MD100-5T) is used, in conjunction with a transimpedance amplifier, to convert the optical signals back to voltages.

- Photodetector size = 1.4mm x 1.4mm
- Photodetector pitch = 1.5mm
- Responsivity of photodetector at $\lambda = 900nm = 0.33$
- Typical rise time of unbiased photodetector = 26ns

The current generated by each photodetector in the array is converted into a voltage by a transimpedance amplifier (National Semiconductor LF333N) designed with a gain of $A_v = 10000$.

The voltage output from the photodetector subsystem for a single digitally-driven VCSEL is shown below. The simulated output from the same subsystem using the analogue driver is also shown. The maximum voltage from a single detector will be equal to 28 times the peak voltage or $V_{peak} = 1V$.

Digital Signal Processor-based Neurons
Neurons are the basic processing elements of the network. They provide a monotonic thresholding function which relates the neuron input to its output. The thresholding function is generally sigmoid-like although other functions (e.g. Mexican hat) can be used.

In addition to the thresholding function, the neuron must be capable of storing the result of the thresholding operation to enable the dynamic alteration of the neuron state.

The digital signal processor board allows the precise functionality of the neuron to be altered with minimum delay. A fully featured software development kit is supplied with each board allowing the neuron to be programmed using a high-level language.
Conclusions

- Assembly of the component subsystems of the neural demonstrator is complete and these subsystems have been fully characterised.

- The demonstrator is significantly smaller than the previous system as well as having greater flexibility of response.

- The characterisation of the subsystems has been used to improve the network simulations allowing accurate prediction of architectural scalability to be made.

- The choice of digital drivers for the VCSEL array appears to offer improved performance over dedicated analogue drivers although final conclusions will only be possible once the experimental system is fully operational.