Optical System and Components for a Terabit/s Optoelectronic Interconnect Demonstrator

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Background

Recent analysis [1] has shown that the i/o requirements of integrated circuits may soon exceed 1 Tbit/s. Transmission of such high data rates by conventional wires is predicted to be fundamentally limited over relatively short distances of the order of centimetres [2]. One possible approach to this problem is to exploit the high space-bandwidth potential of free-space optical interconnects in combination with optoelectronic-VLSI (OE-VLSI) components - surface normal optoelectronic devices integrated with silicon VLSI. A major focus of our work in this area is as part of a collaborative European Commission funded project to construct a packet-switching matrix-matrix optoelectronic crossbar interconnect which aims to demonstrate an internal aggregate connection bandwidth to a silicon VLSI chip in the region of 1 Terabit/s. The system is described in full elsewhere [3,4,5]. In this paper we describe the optical components of this Smart-Pixel Opto-Electronic Connection (SPOEC) demonstrator [6], their completed design and early test results in advance of full system operation.

Optical Layout

The demonstrator system under construction implements a 64x64 optoelectronic cross-bar switch as a technology test-bed. The optical layout is shown in schematic as Figure 1 below. The 64 (electrical) input data streams are converted to the optical domain by an 8x8 array of vertical-cavity surface emitting lasers (VCSELs) operating at 956nm wavelength. A hybrid micro-lens and bulk lens combination collect the emission and collimate it before it is fanned out 8x8 times using a diffractive optical element (DOE 1). The fanned out signals are routed to a hybrid OE-VLSI chip by thin-film beam-steering elements (PBS-A and PBS-B) and an imaging lens (Lens 2). The fan-out results in an 8x8 array of identical images of the input VCSEL array falling on the hybrid InGaAs/CMOS OE-VLSI smart-pixel crossbar array chip. The 64-times fan-out combined with the 250Mbit/s/channel data rate corresponds to an aggregate 1 Tbit/s i/o to this switching chip. The silicon circuitry of the chip implements header-decoding and routing of the data to differential output modulator pairs which are read by a 1047nm wavelength Nd:YLF laser and the reflected data streams are routed using polarisation control to a second hybrid OE-VLSI chip which converts the output data back to the electrical domain.

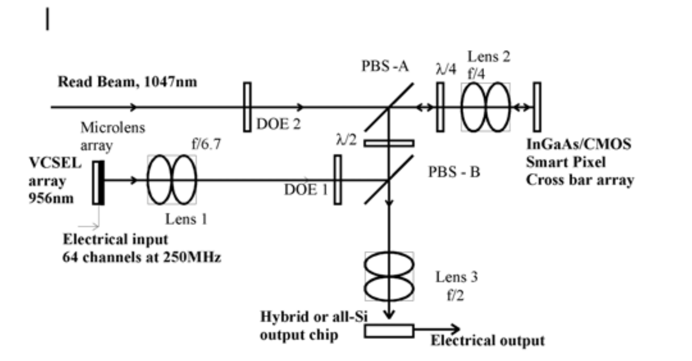

Figure 1 Schematic layout of the SPOEC Demonstrator

Bulk Optical Design and Optomechanics

The relay of information through the system is performed by a set of three custom-designed multi-element bulk lenses (see Figure 1 above). An image of the input VCSEL array is transferred, with demagnification of x1.67, to the switching OE-VLSI smart-pixel chip by a combination of the f/6.7 Lens 1 and an f/4 Lens 2. These two five-element anastigmatic lenses have been based on earlier designs [7] optimised for this application using CODE V® software. The principal challenge to the relay optics arises from the x64 fan-out which leads to a field size of ~17.5mm diagonal at the OE-VLSI smart-pixel chip. In addition to this high field requirement at a wavelength of 956nm, the output of the data from the switching chip modulators is at a wavelength of 1047nm and Lens 2 is must also be well corrected at this second wavelength. The output data path is effected through a further four-element lens operating at f/2 (Lens 3), adapted from a design by Reiley and Sasian [8]. These lenses have all been extensively modelled and, allowing for manufacturing and alignment tolerances, we have been able to specify detector and modulator diameters of only 35µm. The compact (30cmx20cmx10cm) system will be mounted on a slotted baseplate using custom optomechanics to give the required stability.

Diffractive Optics and Hybrid Integration of Micro-Optics

An important challenge in the use of VCSEL arrays as input devices for free-space optical interconnects is the efficient collection of their emission. This is particularly important in a system such as this, where 64 VCSELs are fanned out to 4096 detectors. To maximise the optical power reaching the detectors we have integrated a refractive microlens array (8x8 f/5 lenses operating at f/3) to collect 90% of the emission and reduce its divergence to match the f/6.7 bulk Lens 1. This combination allows efficient collection while retaining the necessary illumination of multiple periods of the diffractive element DOE 1 for efficient fan-out. The packaging scheme is shown in Figure 2. A mounting ring around the VCSEL array provides the correct stand-off with lateral alignment provided in manufacture by the reflection of an alignment laser from diffractive zone-plate lenses included in the corners of the VCSEL array metalisation [9,10].

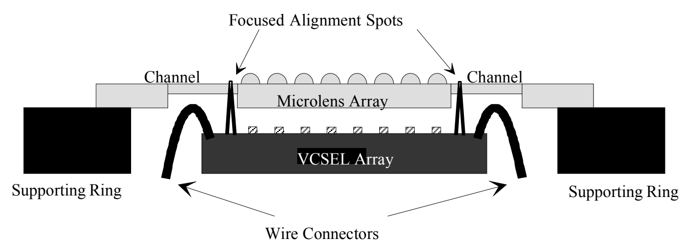

Figure 2 Hybrid alignment and mounting scheme for microlens array on VCSEL array

The 8x8 fanout of the VCSEL emission and the generation of the 8x16 array of read-out beams from the Nd:YLF laser will be performed by binary phase-only diffractive optical elements. Whilst both binary and 8-level elements have been manufactured, initial system testing will use the binary designs, preferred because of their more effective zero-order suppression to ~0.05% (to reduce crosstalk) and low (1-3%) non-uniformity although at some cost in reduced (~60-65%) diffraction efficiency.

Thin-Film Beam Routing Optics

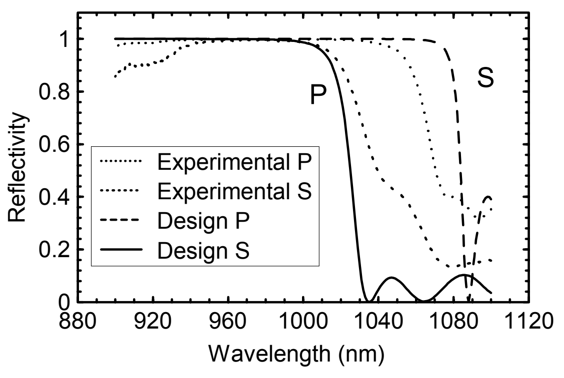

Figure 3 Comparison between experimental spectral performance and design for dual-wavelength thin-film beam-steering elements.

The beam-routing optics in the demonstrator must, as is clear from Figure 1, differentiate between the two wavelengths employed in the system, 956nm and 1047nm. Whilst the 1047nm wavelength read-beam from the Nd:YLF laser is polarised and can therefore be steered using conventional polarisation techniques, the VCSEL array cannot be assumed to be uniformly polarised across the array. Thus the requirement for the beam-routing components is that they act as polarising beam-splitters at 1047nm and simultaneously as polarisation-independent reflectors at 956nm. Particular attention has been paid to the efficiency of reflection at 956nm to maximise transmission of the VCSEL power to the switching chip detectors as discussed above. In addition, these elements (PBS A and B) must operate over an angular range of ±8º around 45º.

The approach that has been taken is to design a thin-film coating [11] on a 45º-angled substrate. The coating that has been fabricated is a 5µm thick, 30-layer combination of TiO_2 and SiO_2 on a B270 substrate. The layers are grown using thermal sources and ion-assisted deposition. The designed and experimental performance of the elements as a function of wavelength is shown in Figure 3. Note the near-100% reflectivity at 956nm and the >2.5:1 contrast at 1047nm. Although this implies some loss for the signals being passed from the modulators on the switching chip to the output chip, this can be tolerated given the generous power budget for this part of the system. The performance of manufactured elements as a function of angle has been measured and has been shown to be sustained over the required range, in particular with the critical reflectivity at 956nm wavelength remaining above 98% over the whole 16º range.

Summary

The optical design of the SPOEC demonstrator system has been successfully completed with the key components shown to perform, individually, as required. The optical power budget shows that the critical requirement of ~7.5µW of optical power at the switching chip detectors will be available to allow the required high data-rate operation. Further work is planned in the areas of optomechanics and integration once the results of system testing are available. The full system testing of this promising technology test-bed will provide valuable insight into the device and integration challenges associated with the construction of Tbit/s scale free-space optoelectronic interconnects.

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