Analysis and Modelling of a 2D Optical Interconnect for Parallel Computing

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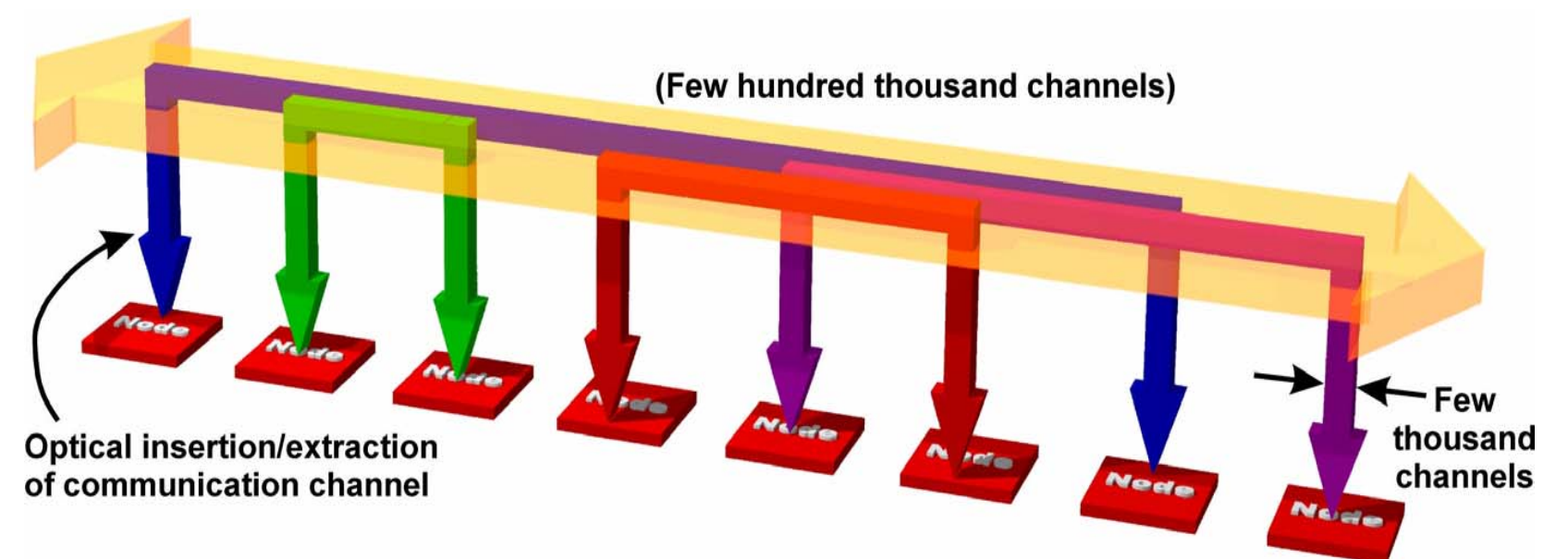
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Why Optics?

- Inherent parallelism

- Higher temporal and spatial bandwidths

- Higher interconnection densities

- Less signal cross-talk

- Immunity from electromagnetic interference and ground loops

- Freedom from quasi-planar constrains

- Lower signal and clock skew

- Lower power dissipation

- Larger number of fan-ins fan-outs

- Potential for reconfigurable interconnects

(Few hundred thousand channels)

Optical insertion/extraction of communication channel

Few thousand channels

'Optical Highway' carrying hundreds of thousands of channels linking non-local nodes with thousands of channels
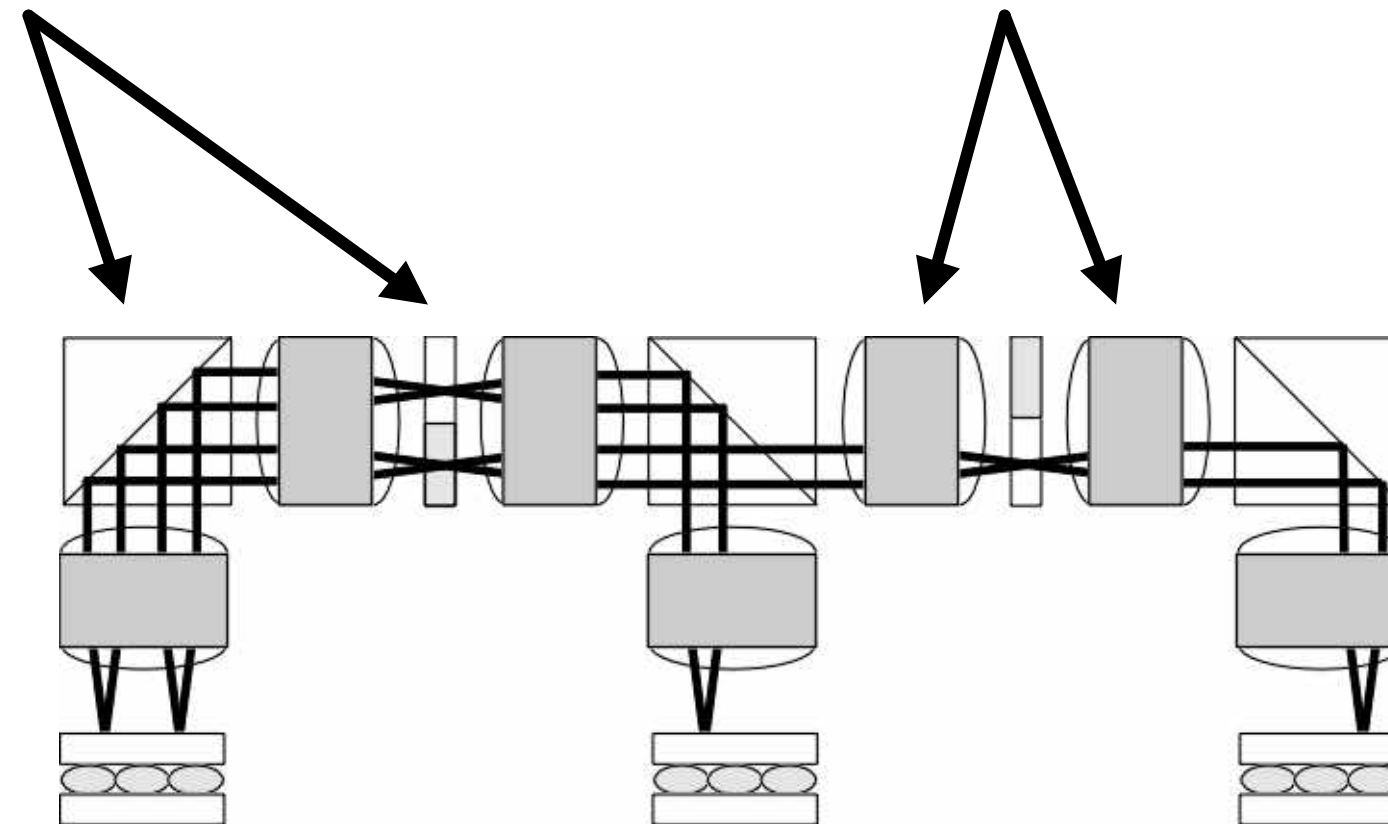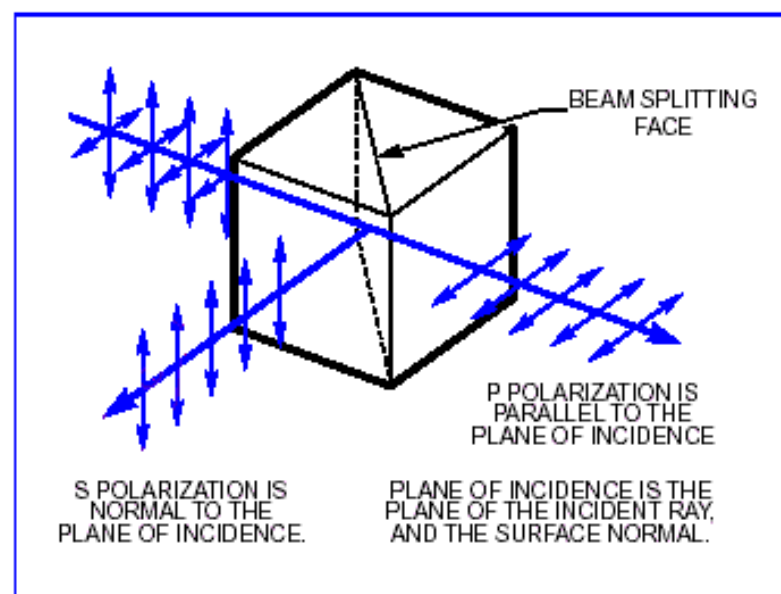
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Technologies - Free Space Optics

Polarisation Beam Splitters (PBS)

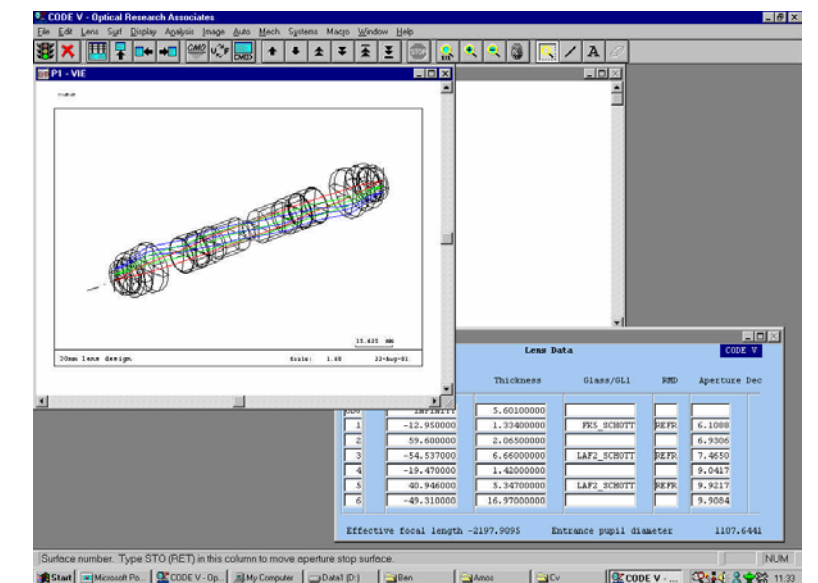Used to route data streams into and out of Optical Highway.

Patterned Birefringent Plates are used to selectively flip polarisations of the beams to be routed out of the Optical Highway.

Lens

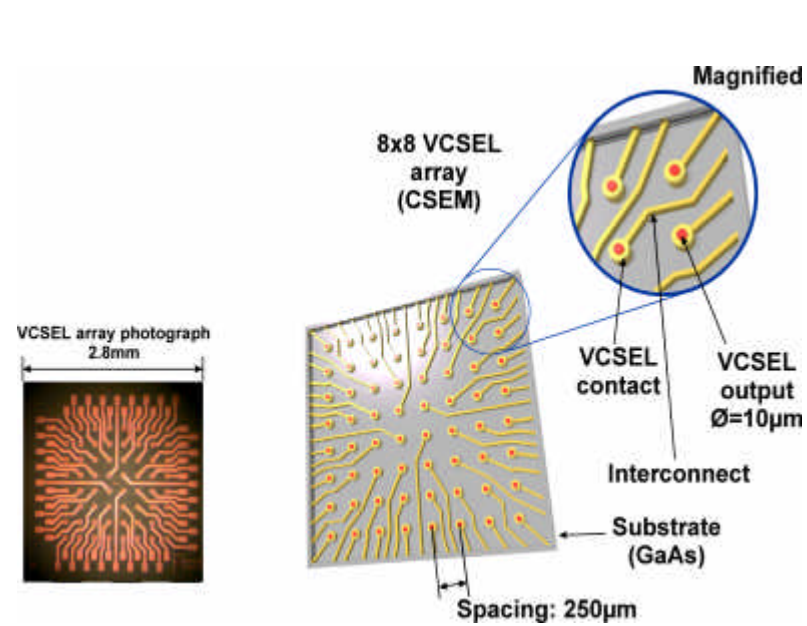Combination of bulk and micro lenses could be used

Code V simulations to insure aberration limited spot size small enough to eliminate cross-talk between channels. Model developed to generalise to multiple relay stages.
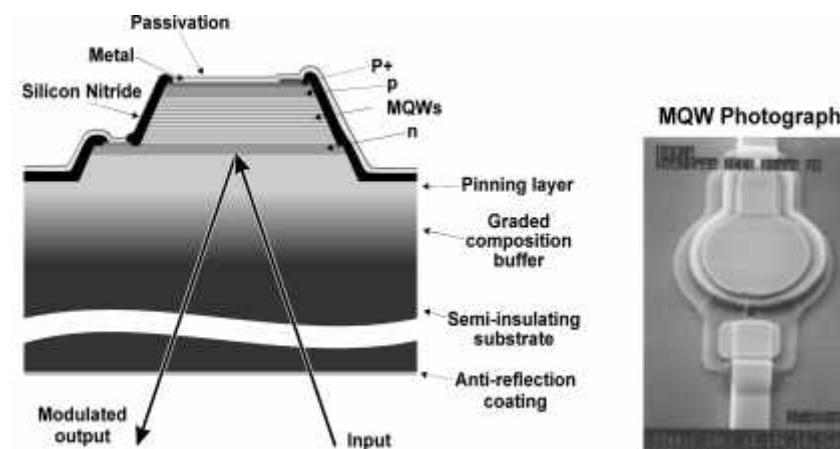

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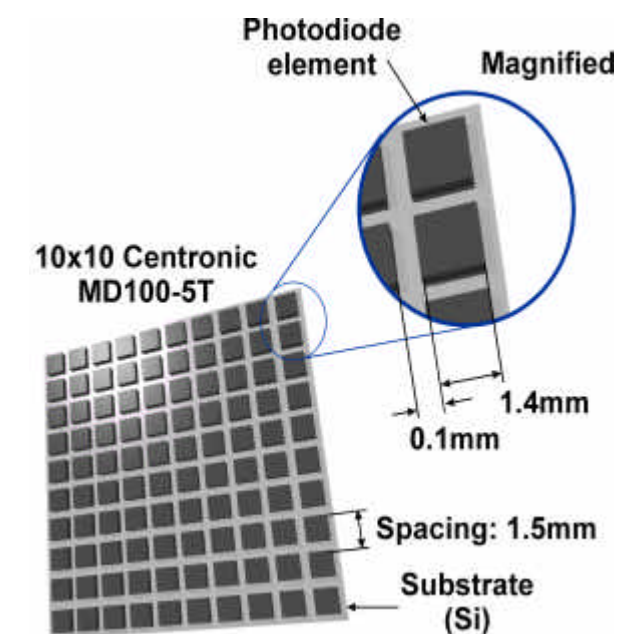
Technologies - Smart Pixel Array

8x8 VCSEL array (CSEM)

Magnified

VCSEL array photograph 2.8mm

VCSEL contact

VCSEL output Ø=10µm

Interconnect

Substrate (GaAs)

Spacing: 250µm

VCSEL - Light Source

Passivation

Metal

Silicon Nitride

P+
p
MQWs
n

Pinning layer

Graded composition buffer

Semi-insulating substrate

Anti-reflection coating

Modulated output

Input

MQW Photograph

Modulator - Data Transmission

Photodiode element

Magnified

10x10 Centronic MD100-5T

1.4mm
0.1mm

Spacing: 1.5mm

Substrate (Si)

Detector - Data Reception

Arrays of optical components fabricated in a suitable optically active material are 'flip-chip' bonded to a silicon processing layer.

Modulators have a number of advantages for bonding to silicon especially in thermal dissipation.
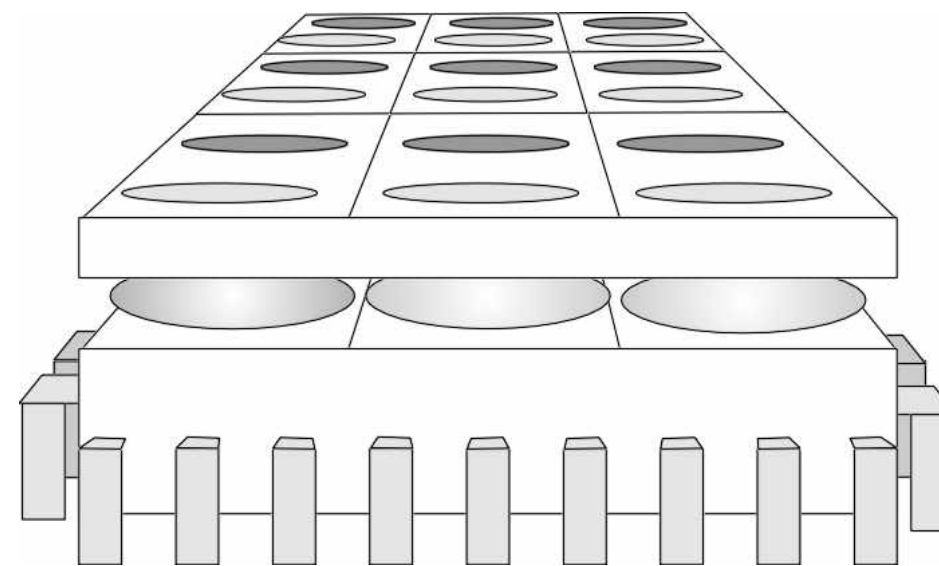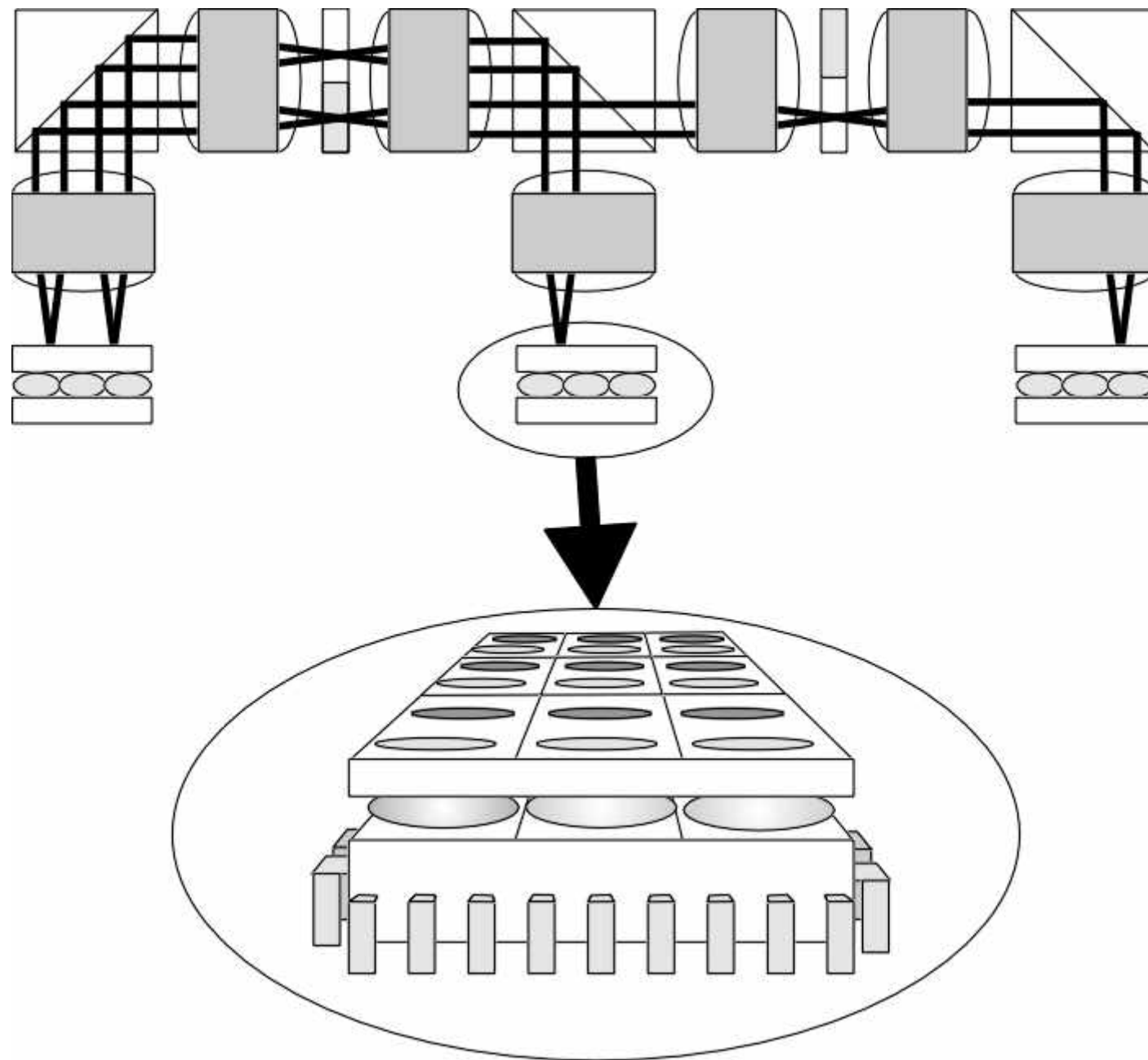
Silicon layer may be conventional VLSI silicon or FPGA (Field Programmable Gate Array) for reconfiguration.
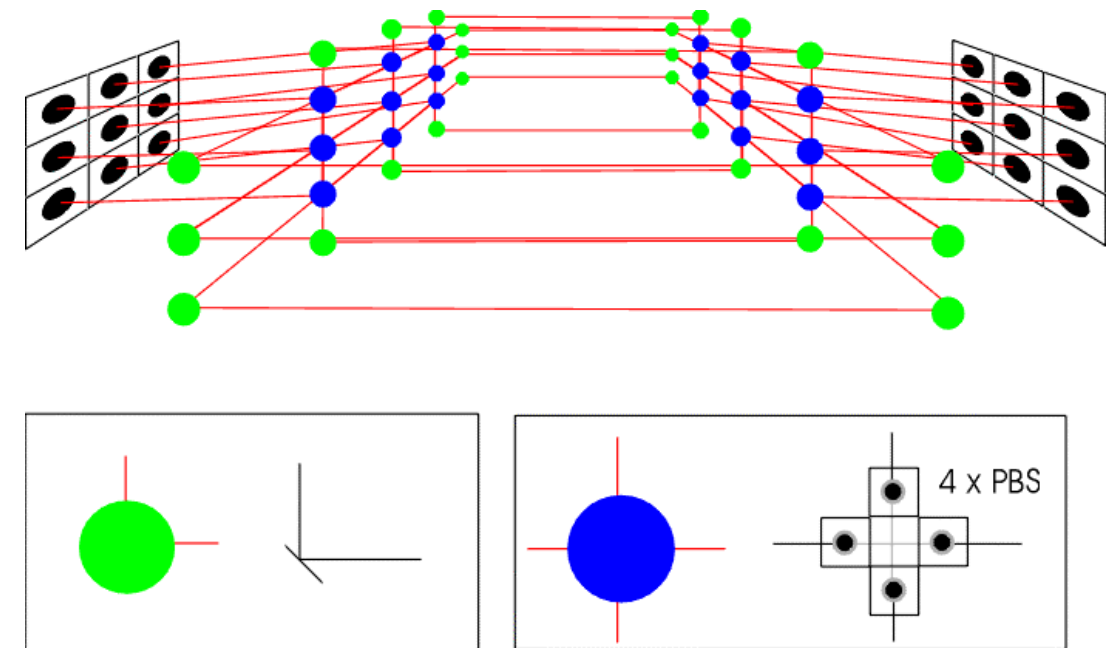
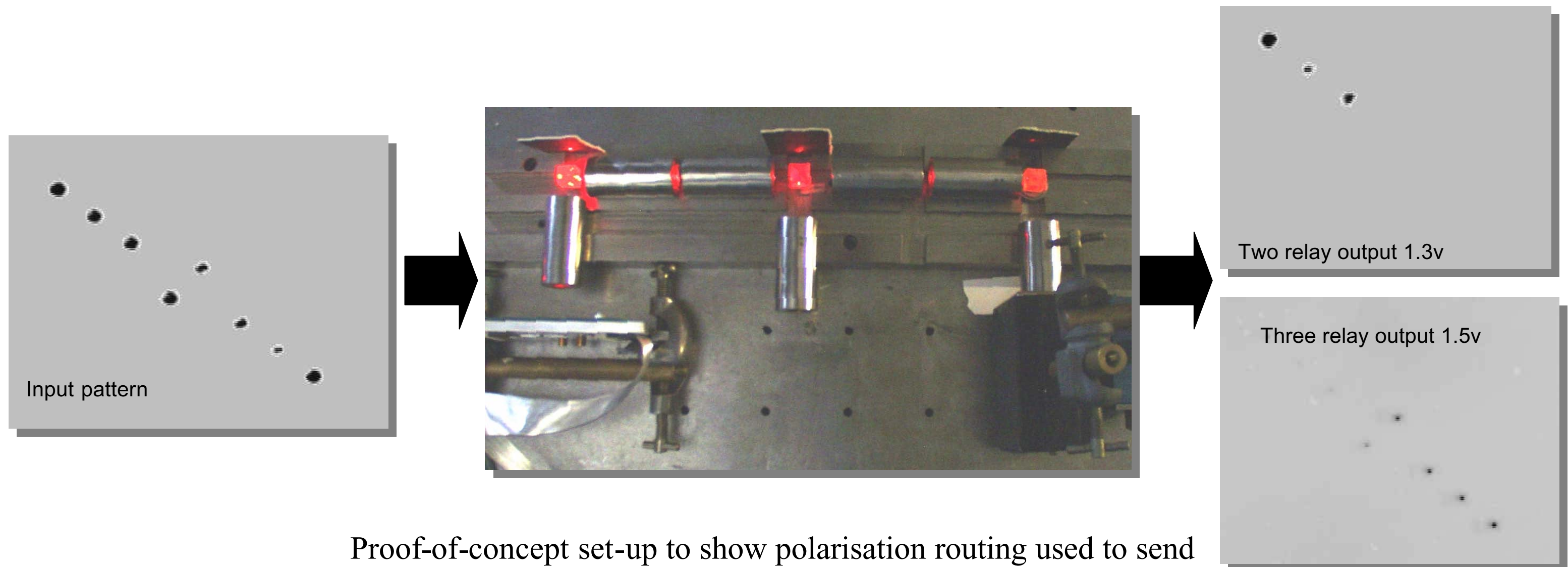Silicon can be used for routing or fine grained processing

Physical Layout

- Data channel hard 'wired'

- Polarisation used to control optical path

- Wrap-around links used at ends of each dimension to condense package and reduce optical path length

- 18 node layout shown below

4 x PBS

Experimental Optics Set-Up

Input pattern

Two relay output 1.3v

Three relay output 1.5v

Proof-of-concept set-up to show polarisation routing used to send signal beams from VCSEL array to CCD cameras.

Used to help develop models of the optics and obtain perimeters used in later modelling of the system.

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Modelling

- Analytical model

- Equal Bandwidth Methodology

  ➢ Longer length links require more channels as bandwidth decreases with optical loss

  ➢ Requires multiple clock speeds across optoelectronic interface chip

- Link bandwidth assume to be receiver limited

- SPA silicon only used as routing / traffic controller

- Simulation / Experimentation required to validate model

$$B_{optical} \leq \frac{1}{4} f_o N \left[\frac{\xi^X (1-\xi)}{1-\xi^X} \right]$$

$$L_{optical} \approx \frac{q\sqrt{p}}{2c} + 40 \times 10^{-9}$$

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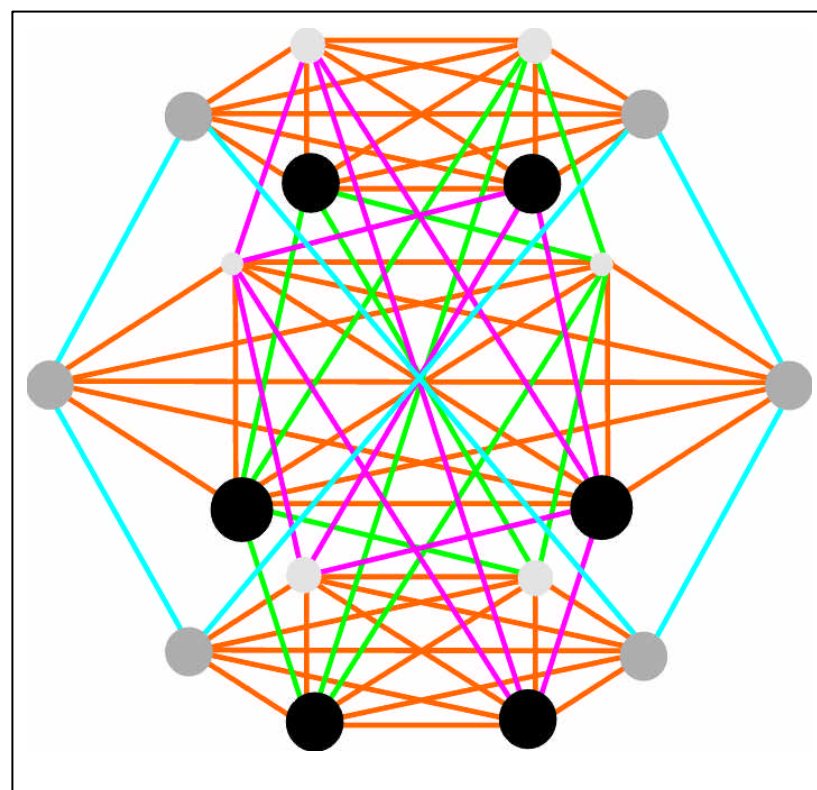
Comparison of Results
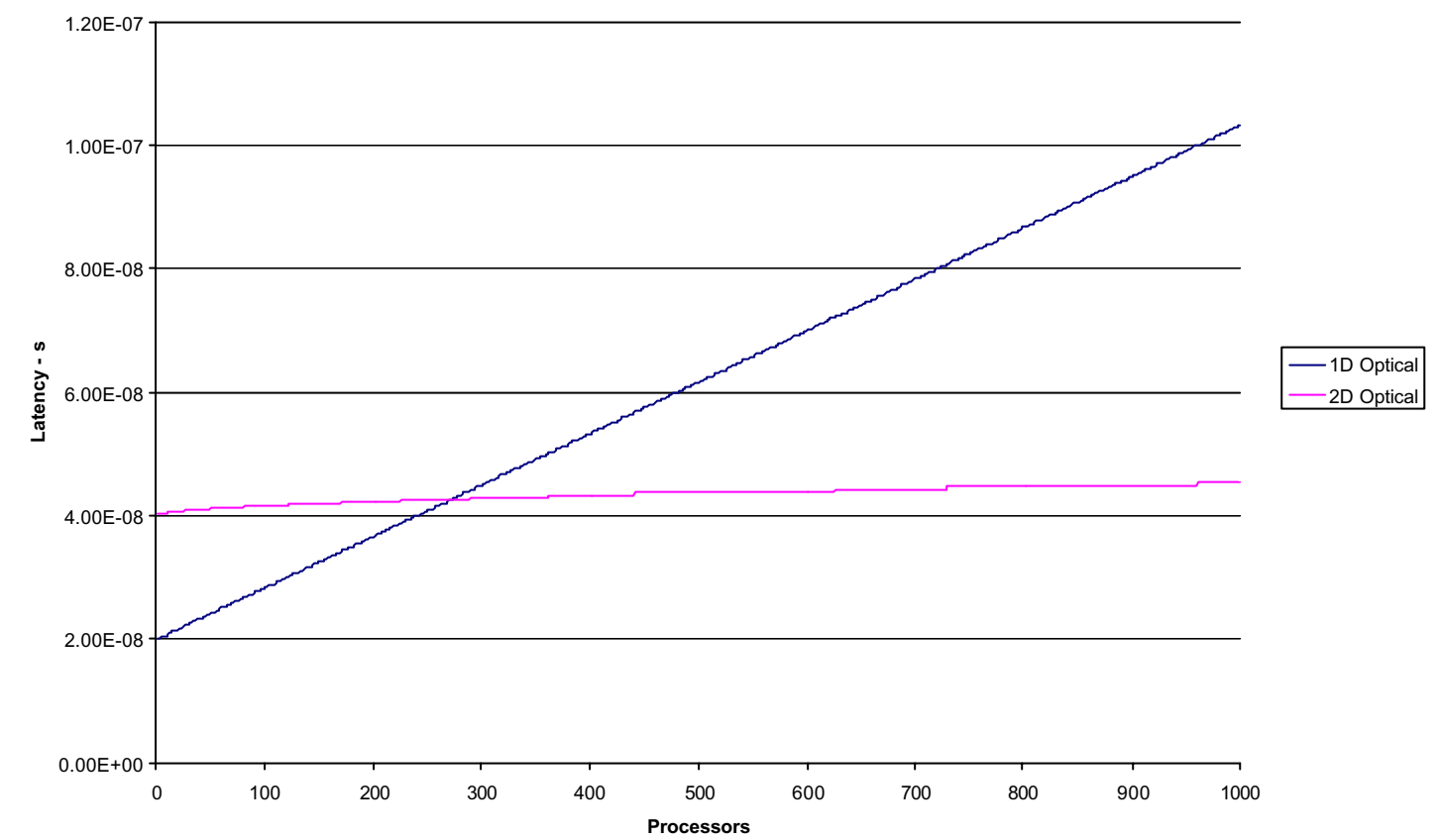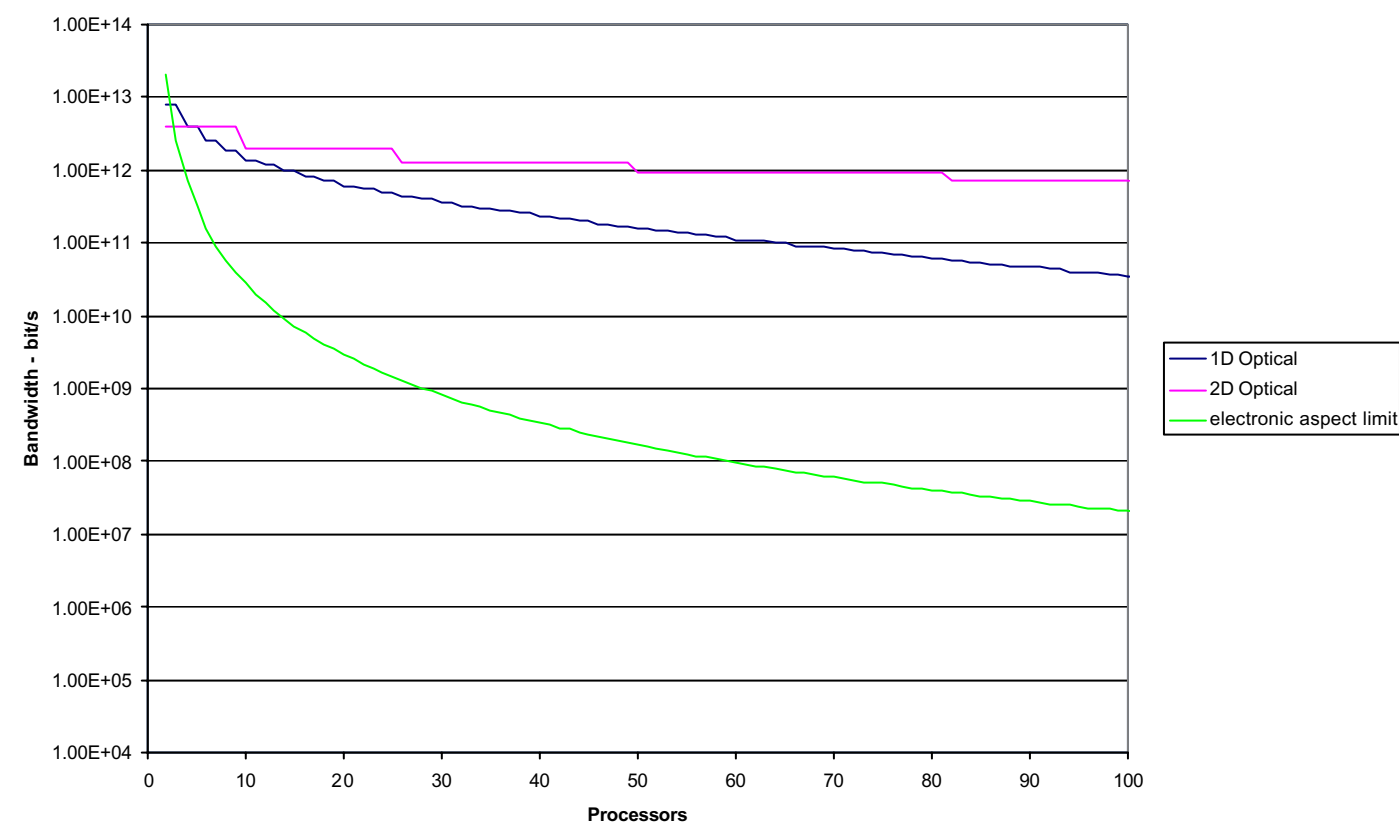
2D Optical Interconnect compared with analysis of 1D Optical Interconnect and Aspect limited electronic interconnect assuming equal silicon area as basis.

Computational Issues of 2D Architecture
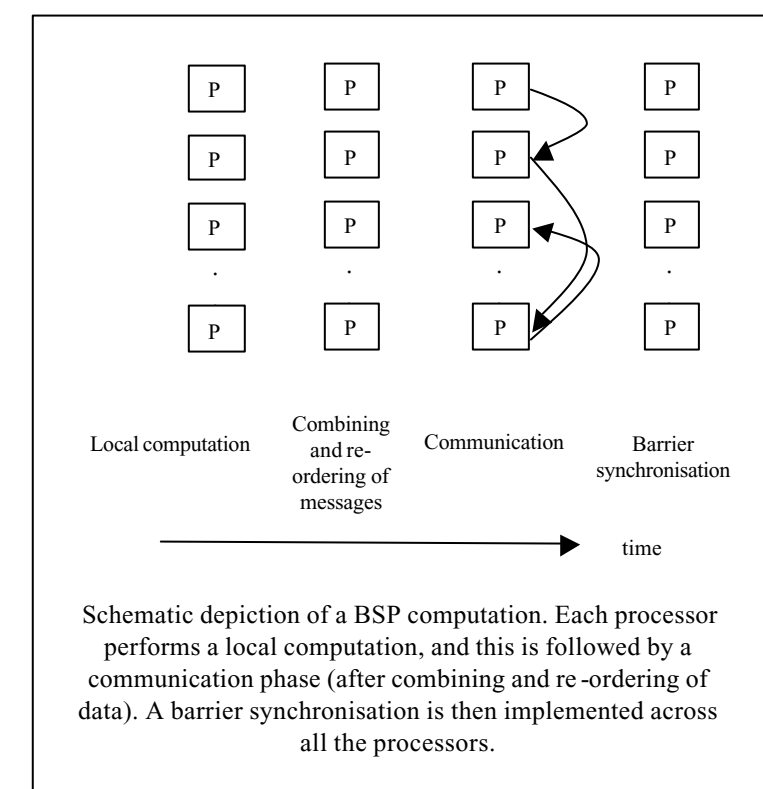
Architectural Issues

• High connectivity (e.g. completely connected network or hyper-cube like), below
•Large buffers in smart-pixel layer

Algorithmic issues

•Algorithms designed to allow communication of large messages (to exploit optical bandwidth)
•Messages collected in smart-pixel layer prior to inter-processor communication.

Initial performance results, based around an implementation of the Bulk Synchronous Parallel model indicate potential for substantial performance enhancement for communication intensive problems. Examples of such problems are parallel sorting, graphics and FFTs.

| P | P | P | P |

Local computation | Combining and re-ordering of messages | Communication | Barrier synchronisation

time

Schematic depiction of a BSP computation. Each processor performs a local computation, and this is followed by a communication phase (after combining and re-ordering of data). A barrier synchronisation is then implemented across all the processors.

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Conclusions, Research Areas and Further Work

•2D interconnect can provide high bandwidth, highly scalible communications for massively parallel computers.

•Latency penalties from optics to electronics domain changes are of set by smaller routing costs of the more direct connections available optically.

•High bandwidth required for communications bounded problems and to service the data requirements of faster processing.

Research Areas and Further Work

•Large, reliable arrays of optoelectronic components (>128x128).

•Integration with silicon technologies (bonding techniques or silicon devices).

•Efficient thermal engineering.

•Simulation of real traffic patterns on interconnect.

•Topology of interconnect and components.

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