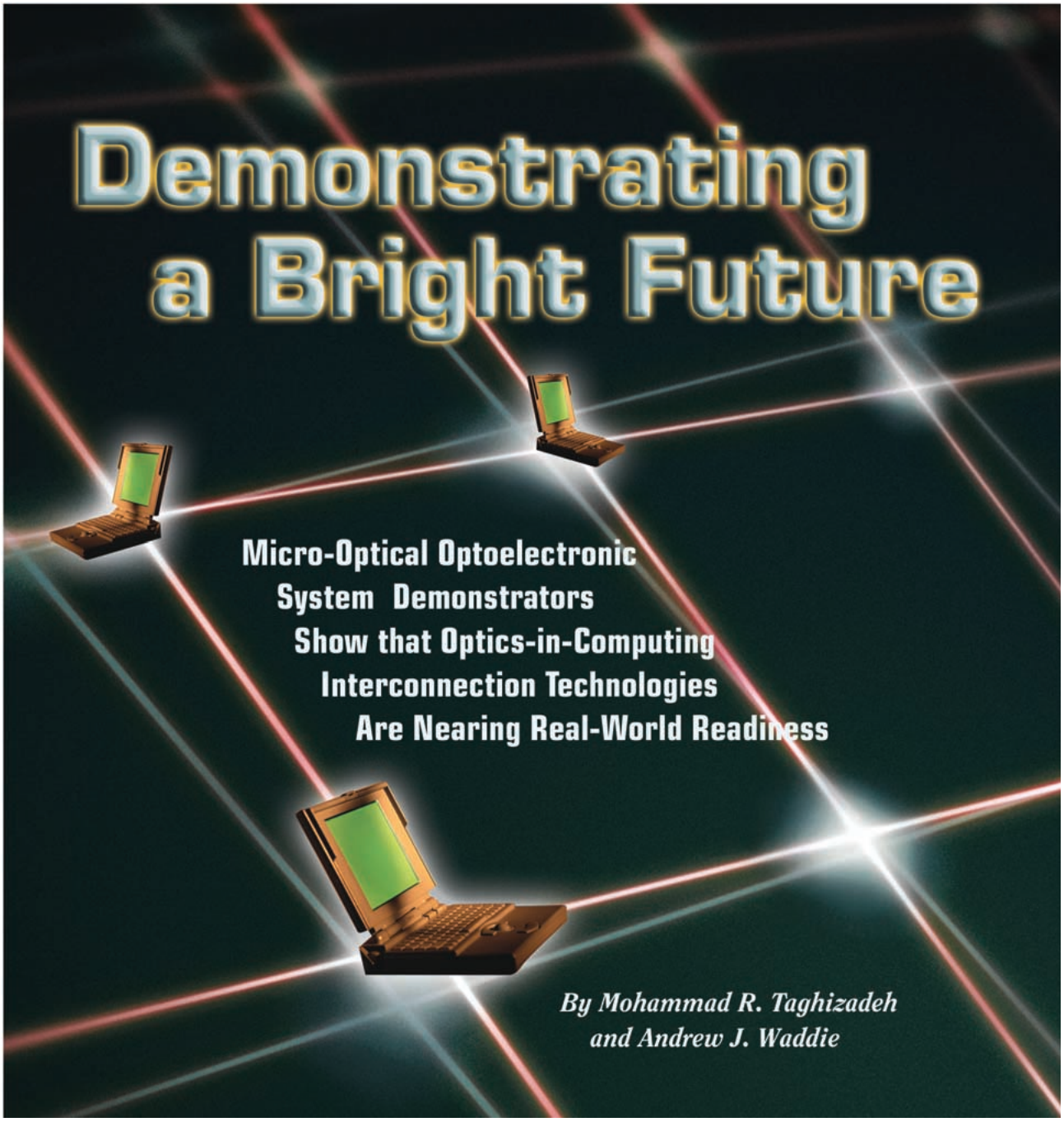

One side effect of the information technology explosion of the past decade has been the increasing relevance of research into optical interconnection methods and technologies. It is predicted that of the various technological impediments facing the information technology industry, bandwidth will have the most significant impact upon the ever-increasing power of both computers and the Internet. Above a certain clock rate, conventional electronic circuits are incapable of sufficiently reliable operation and some form of noninterfering transmission architecture must be used. Optics has long been proposed as a suitable technology for the implementation of such a low-interference, high-reliability architecture at both the intra- and inter-computer levels.

The last several years have produced significant advances in the design and fabrication of optoelectronic device arrays. They have been fabricated in ever larger two-dimensional (2-D) arrays with improved device uniformity and reduced device power consumption, allowing realistically sized optics-in-computing systems to be assembled. Concurrently, the VLSI technology advances that have driven the improvements demonstrated by

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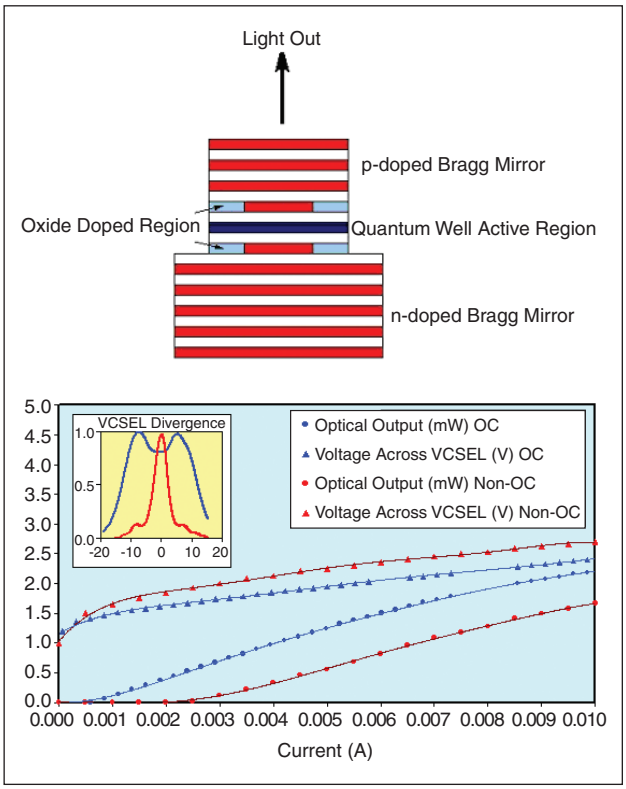
conventional Si-based electronics have percolated through to the fabrication of micro-optical components. These techniques allow the fabrication of large, highly uniform, free-space optical interconnections, permitting the creation of optoelectronic demonstrator systems of increasing complexity and power. In this article we shall describe two different optoelectronic architectures that have been designed and constructed at Heriot-Watt University as well as outline those areas of the optical/optoelectronic interconnection technology that we feel have the greatest potential for future exploitation.

Optoelectronic Device Arrays

Optoelectronic devices can be divided into two broad categories—active, where the devices generate and modulate their own optical signal (e.g., vertical cavity surface-emitting lasers [1]), and passive, where an externally supplied optical signal is modulated in some way (e.g., electro-optic effect devices [2]). Significant improvements in operating characteristics (i.e., reduced electrical power consumption, reduced bias voltage, reduced threshold current, and increased responsivity) have been made to both classes of device. The greatest improvements have been made to active devices, which has meant they have become the preferred optical modulation device in optoelectronic systems, although passive devices are still used as photodetectors. Wavelength coverage from active devices is generally good, although there is still a relative paucity of microlasers capable of operating at the standard telecommunications wavelengths of 1.3 μm and 1.55 μm. The microlasers used in the optoelectronic demonstrator systems described in this article operate in the near-IR (800-1000 nm) and are based around GaAs/AlGaAs quantum-well devices.



1. Vertical cavity surface-emitting laser. Schematic of device structure and operating current and optical power/voltage curves.

Figure 1 shows a schematic layout of a vertical cavity surface emitting laser and the current-power characteristics of two different VCSELs supplied by Avalon Photonics. The first of these VCSELs has an Al_xO_y confinement ring [3], produced by the diffusion of oxygen into the first AlAs layer of the DBR mirrors, resulting in a lower threshold current, greater wallplug efficiency, and longer device lifetime. However, the presence of the oxide confinement layer causes a significant degradation in the output mode quality compared to a nonoxide VCSEL, as shown by the inset in Figure 1. The second VCSEL, which is an older device lacking these oxide confinement layers, was initially used in both demonstrator systems outlined in this article. The poor lifetime exhibited by the non-oxide confined (OC) VCSELs (as low as 10 hours in some cases) resulted in their replacement with the OC-VCSELs despite the poor mode quality exhibited by the OC devices.

Micro-Optical Interconnection Elements

A micro-optical (or diffractive optical) element is a representation of an optically thin phase-only hologram such as a surface-relief profile [4]. It is the preferred method of generating highly uniform, arbitrary free-space optical interconnections between optoelectronic modulators and detectors [5], [6]. The micro-optical technology evolved from the field of optical holography, in part due to the significant increases in the processing power of computers during the 1980s and the 1990s, although the difficulties associated with the creation of optical holograms was also a significant factor in their adoption for optics-in-computing demonstrators. Using standard optimization techniques, high-efficiency (>70%), low-nonuniformity (<1%), nonlocal interconnections can be designed and fabricated using conventional VLSI techniques. The fabrication of the micro-optical or diffractive element is a realization of a phase-only, complex-amplitude transmission function (i.e., a description of a thin phase hologram) as a refractive index modulation in an appropriate substrate material. Microlithographic techniques are used to create the refractive index modulation as a surface relief profile leading to either a continuous or, more commonly, quantized surface profile [7]. The element is fabricated by a combination of a photolithographic patterning stage, where a photoresist-coated substrate is patterned using a contact printing process, and a reactive-ion etching (RIE) pattern transfer stage, where the photoresist pattern is transferred into the substrate. A more detailed description of the fabrication process can be seen in Herzig et al. [8]. The binary amplitude mask used to produce the patterned photoresist is written on a chrome-on-quartz substrate using an electron-beam writer at a resolution of 0.1 μm and for feature sizes ≥ 2 μm. This mask is then transferred into an appropriate substrate at a comparable resolution. The pattern transfer depth can be controlled to within ±2 nm over an area of ~1 cm^2 or to within ±5 nm in general. In order to realize the refractive index modulation as a surface relief profile, the surface

relief depth must be appropriate for the mode of operation of the element; i.e., either reflective or transmissive. The etch depth for a π phase delay in a substrate of refractive index $n(\lambda)$ is equal to

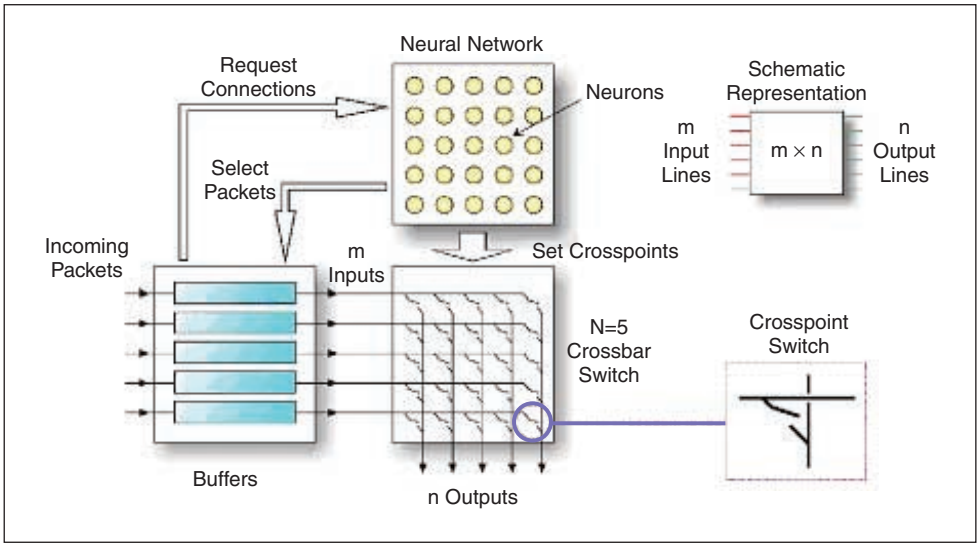
$$d = \frac{\lambda}{2(n(\lambda)-1)}.$$

For a near-IR element, the typical etch depth for a binary element fabricated in fused silica is 1.0-1.5 μm for a π phase step. The aspect ratio of the features of a typical fanout element is of the order of 2-4, which is well within the achievable aspect ratio for the reactive ion etching procedure.

The Hopfield Network Demonstrator

The Hopfield network demonstrator [9] is designed to perform a crossbar switch throughput optimization. Figure 2 is a schematic of the system that this network operates in.

Incoming data packets, which consist of an output address header and data payload, are queued in the input buffers. The output address header of each incoming packet is decoded by the queue manager for that input line to generate the appropriate interconnection request. The request vectors of all the input queue managers provide the initial state of the Hopfield network, which has one neuron corresponding to each cross point in the crossbar switch. The Hopfield network is allowed to evolve to a steady state that will generally produce an optimal configuration for the crossbar switch. The cross points corresponding to the on-neurons in the Hopfield network are closed and each queue manager transmits the appropriate packet through the crossbar switch. The request vectors of the queue managers are then updated and the cycle can be repeated. The throughput of the switch is said to be optimized if the number of packets selected for transmission by the Hopfield network on any one switch cycle tends to $\min(N_I, N_O)$.

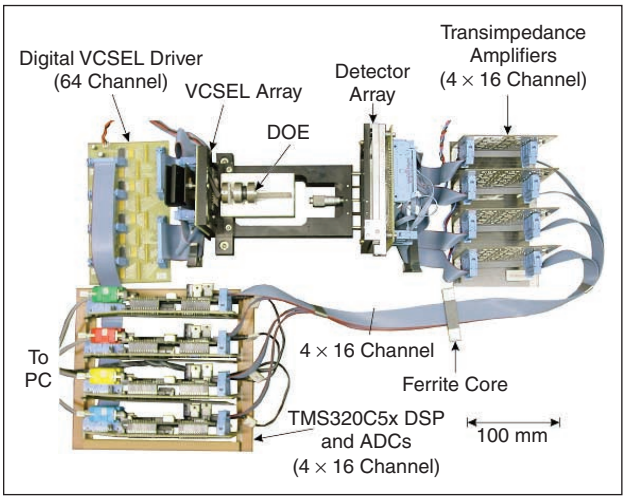


2. Hopfield neural network switch controller.

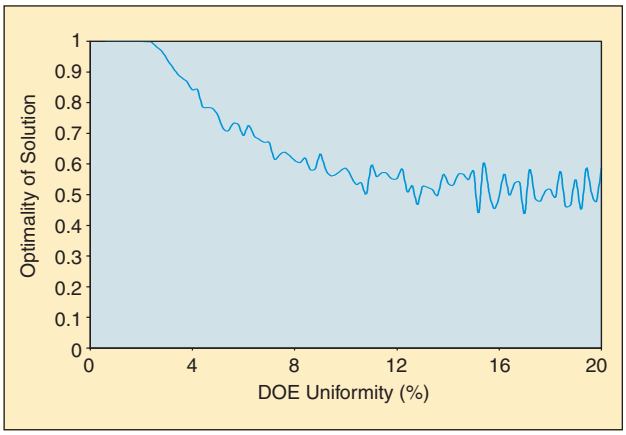
The Hopfield neural network [10], which controls the setting of the crossbar switch as described above, is implemented using free-space optical interconnections in conjunction with arrays of optoelectronic devices and is shown in Figure 3.

The optoelectronic devices provide the electronic-optic and optic-electronic interfaces to the diffractive optical-element-based free-space interconnection. The electronic-optic interface consists of an 8×8 array of OC-VCSELs supplied by Avalon Photonics with appropriate analog ASIC drivers. The optic-electronic interface is an off-the-shelf Si photodetector array with a transimpedance amplifier to produce the correct voltage levels for application to the neurons. The neurons themselves are implemented electronically using Texas Instruments digital signal processors, each of which provides the functionality for 16 neurons.

A micro-optical element provides the inhibitory interconnections between the neurons. The interconnection required for the $N \times N$ crossbar switch throughput optimization problem is an equal-arm cross with N–1 orders in each arm and with the central zeroth order suppressed. The diffractive optical element (DOE) was designed using a combination of an iterative Fourier transform algorithm (IFTA) and a closed-form trapezoidal algorithm. In general, these standard design methods allow the creation of DOEs with efficiencies of greater than 70% and reconstruction errors of less than 1%. However, due to the restrictions placed upon the DOE period by the optical system, a reduction in the overall efficiency of the DOE to 50% was required to ensure that the nonuniformity was of an acceptable



3. Hopfield neural network optoelectronic demonstrator.



4. Optimality of solution for 8 × 8 optoelectronic Hopfield network.

level (< 1%) and that the SNR between the "on" and "off" orders was greater than ten.

The VCSEL arrays used in the Hopfield network demonstrator are 8 × 8 arrays (250 μm pitch) supplied by Avalon Photonics. The original (non-OC) microlasers used in the demonstrator emit in the near infra-red (λ = 960 nm) at a divergence angle of 12° FWHM. The average threshold current of the microlasers is 2.65 mA and the average peak power-conversion efficiency is 6.3%. The ASIC CMOS current drivers in Figure 3 supply a maximum current of 3.5 mA at 2 V producing an optical output of 200 μW. The optical output in each channel can be improved by the use of OC VCSELs, which exhibit a significantly higher conversion efficiency, lower threshold current, and improved operating lifetime. This last factor has become significant during the assembly of this demonstrator as the original (non-OC) VCSEL array ceased laser operation during testing of the VCSEL driver circuits. The average threshold current of the OC VCSELs is 0.74 mA with an average peak power-conversion efficiency of 14.3%. Simulations of the current driver circuits with these VCSELs have demonstrated that a maximum current of 4 mA at 2 V is achievable, corresponding to an optical output of 1 mW. The maximum optical power incident upon a single photodetector from one VCSEL is equal to

$$P_{\text{detector}} = \frac{\eta P_{\text{VCSEL}}}{4(N-1)}$$

where η is the overall efficiency of the interconnection element (0.5 in this case), N is the number of input/output channels in the system, and P_{VCSEL} is the maximum optical output from the VCSEL. For the demonstrator system described here, the maximum power per detector is 3.57 μW for the non-OC VCSELs and 17.86 μW for the OC VCSELs. The photodetector array, which is an off-the-shelf Si array, has responsivity at 960 nm of 0.35 A/W, producing a photocurrent of 1.25 μA with the non-OC VCSELs and 6.25 μA with the OC VCSELs. A discrete component amplifier has been designed to convert this photocurrent into a voltage for application to the DSP-based neurons. The amplification factor of this amplifier was determined by calculating the maximum photocurrent that can be generated by one photodetector and equating that photocurrent with a voltage swing of 1 V. The total number of VCSELs that can communicate with a single photodetector is $2(N-1)$, giving a maximum generated photocurrent of 17.5 μA/87.5 μA (non-OC/OC VCSEL). This driver-emitter-detector system has demonstrated successful operation at a modulation frequency of up to 10 MHz.

The demonstrator has not to date been operated; however, each of the individual modules has been operated and characterized. These characterization studies have enabled accurate simulations of the network to be performed. An example of such a simulation is presented in Figure 4. In this set of simulations the tolerance of the network to nonuniformity in the optical interconnection is analyzed. The optimality of solution provided by the network is equal to 1 if every one of the test set of input requests generates the maximum number of outputs (8 for this case).

Simulations of different sizes of network have allowed some estimate of the maximum size of network that can be implemented using the current micro-optical element fabrication techniques. The assumption is made that once a network drops below an optimality of solution of 0.9 it is no longer operating with sufficient efficiency. For this level of acceptability, the maximum allowable interconnection nonuniformity is given by

$$\Delta r_{\max} = \frac{100}{AN + B}, \text{ where } N \text{ is the size of the network.}$$

The network hardware used in the demonstrator gives values of the coefficients in the above equation of $A = 3.287674$ and $B = -1.434819$. For the current state-of-the-art DOE fabrication technology, this result implies a maximum Hopfield network size of ~30 × 30 neurons.

The Smart-Pixel Optoelectronic Crossbar (SPOEC) Demonstrator

The second demonstrator system considered in this article is a packet-switched optoelectronic matrix-matrix crossbar based around a InGaAs detector/modulator smart-pixel [11], where conventional Si-based electronics are combined with optoelectronic devices by means of flip-chip bonding. The system, shown in Figure 5, was designed to demonstrate the feasibility of a >1 Tb/s aggregate bandwidth switch using currently available optoelectronic technology.

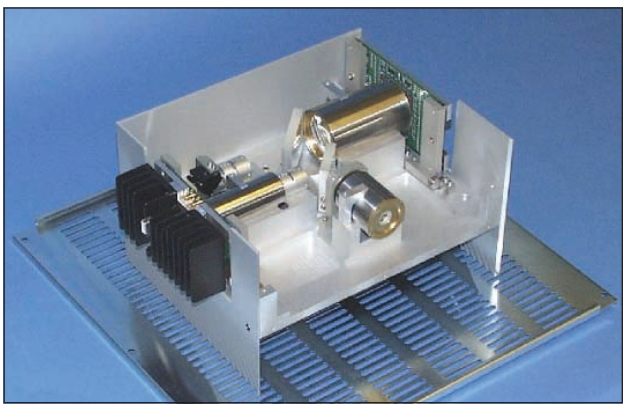
Sixty-four electrical signals are converted into optical signals by an electrically addressed 8 × 8 VCSEL array. Each of the 64 optical outputs from the array are themselves fanned out 64 times by an 8 × 8 fan-out DOE. The resulting set of 4,096 optical signals is relayed to a hybrid InGaAs/Si OE-VLSI chip, which is partitioned into 64 blocks or "super-pixels." Each super-pixel receives the full set of 64 optical input signals and converts these into electrical signals that are electrically routed by the Si-based electronics. The unique output from each super-pixel, which represents the one signal selected from the original set of 64, is converted back into an optical output by means of a differential

pair of multiple-quantum-well modulators. The system is designed as a packet switch with the routing chip configured by the packet header. There are two distinct optical pathways in the demonstrator, the first at $\lambda = 960$ nm is used for data input and the second at $\lambda = 1047$ nm is used for data output. The DOEs used in the SPOEC demonstrator are an 8×8 (data-in optical pathway) and an 8×16 (data-out optical pathway) binary even-orders-missing (EOM) fan-out. The EOM geometry is used because it gives excellent zeroth diffraction order suppression and significantly speeds up the DOE optimization procedure. For example, the 8×8 fan-out element used in the demonstrator system has a period of 72 μm with a minimum feature size of 2 μm, and the diffraction efficiency of the element is 71% with a reconstruction error of <0.5%.

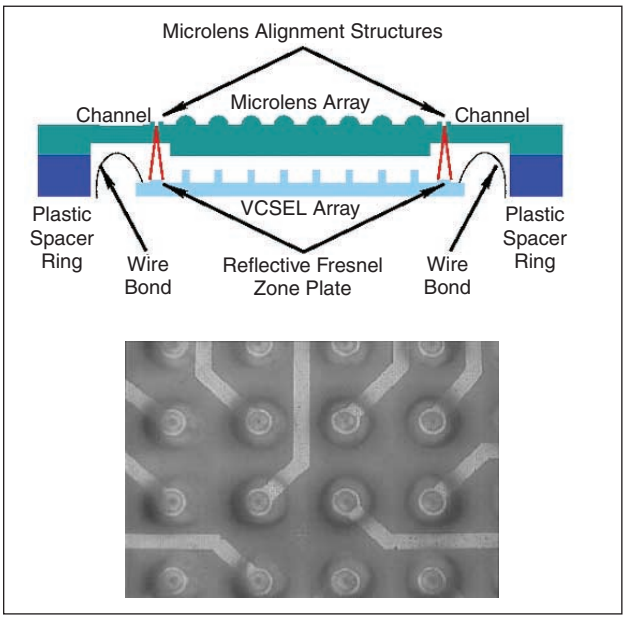
The OC-VCSELs [12] used to supply the optical input data to the system, which are of the same type as those used in the Hopfield network demonstrator, have a large beam divergence (~20°) due to the small size of the laser cavity. This large divergence is reduced, by means of a refractive microlens array, to keep the design tolerances on the bulk optical elements within reasonable bounds. The VCSEL outputs are not collimated to ensure that a sufficient number of periods of the DOEs (typically 3×3) are illuminated to give a uniform fan-out pattern at the smart-pixel array. Figure 6 shows the patented method [13] used to ensure that each microlens is centered on the appropriate VCSEL.

Reflective Fresnel zone plates are placed around the VCSEL array during fabrication and rings are etched onto the microlens array in positions corresponding to the optical axes of the zone plates. During assembly of the hybrid VCSEL/microlens array, the reflective zone plates are illuminated, and once each of the rings on the microlens array has a focused spot in it, the arrays are aligned with each other. The VCSEL-lens separation is controlled by means of a plastic alignment ring of the correct thickness being placed around the VCSEL array. This also provides a convenient platform for securing the microlens array to the VCSEL array. This method has been used successfully to reduce the FWHM divergence angle of the OC-VCSEL by approximately a factor of 3 (from a divergence of ~20° to ~7.5°).

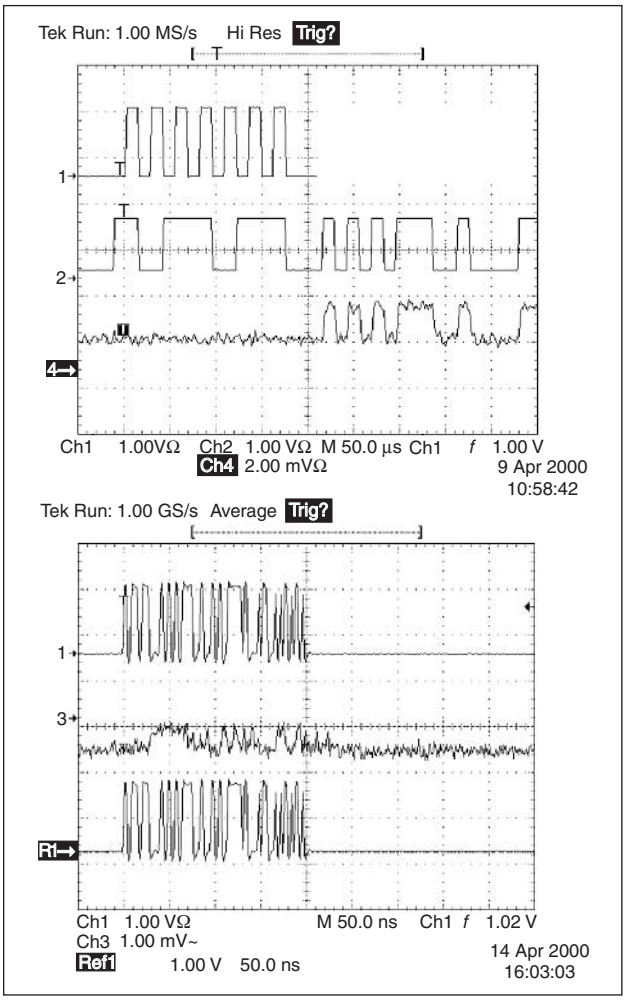
The fully assembled SPOEC demonstrator has been shown to be capable of correctly routing data through the crossbar for a single channel. The maximum routing frequency achieved to



5. The SPOEC demonstrator system



6. Microlens alignment technique used to reduce divergence of oxide-confined VCSEL array.



7. Optical signal routing by the SPOEC system demonstrator. The top trace has a clock rate of 1 MHz, and the lower trace has a clock rate of 125 MHz.

date is 50 Mbit/s for the system operating with fully fanned-out VCSEL signals and 250 Mbit/s for the system operating without VCSEL fan-out. With the fully fanned-out VCSEL signals the calculated aggregate bandwidth of the crossbar is 0.2 Tbit/s. Figure 7 shows two sample routing demonstrations: the first uses the fully fanned-out VCSEL signals and the second shows the routing with the VCSEL fan-out omitted.

The output trace from the lower clock-rate experiment clearly shows the successful decoding of the optical header information and the successful routing of the data portion of the optical signal to the appropriate output channel. The display of the high-frequency results is limited by the output detector noise and the oscilloscope sampling frequency.

Conclusions

In this article we have reviewed the technologies behind two successful optoelectronic demonstrator systems [14]. These demonstrators show that the optics-in-computing technologies are reaching a level of sophistication where their deployment in "real-world" computing/networking environments becomes increasingly likely. The primary requirements for the successful transfer of these technologies from the laboratory to the "real world" are larger, more uniform arrays of the optoelectronic devices and highly stable optical and optomechanical assemblies.

The advent of high-efficiency, low-power consumption arrays of oxide-confined VCSELs has reduced the overall optical complexity of these demonstrators with subsequent gains in the mechanical stability of these optical systems. Although at present the maximum array size of VCSELs that is readily available is 8×8, there is, in principle, no reason why larger arrays cannot be developed.

In tandem with these developments in the optoelectronic device arena, the design and fabrication of micro-optical elements has reached the stage where they can be regarded as the standard optoelectronic interconnection method. Although there are some cases where guided-wave interconnections are necessary and/or advantageous, for most optics-in-computing systems the sheer flexibility of the free-space micro-optical technology ensures its dominance. Over the next ten years we envisage the trickle down of improved VLSI fabrication techniques from electronics to micro-optics. This, in conjunction with the advances in raw computational speed, will allow the creation of larger and more complex interconnections with greatly improved uniformity of output.

As this article went to press, our neural network demonstrator became fully operational, and full experimental results will be appearing in various journals shortly.

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