Optoelectronic Neural Networks for Switching

Heriot-Watt University Edinburgh

M. R. Taghizadeh, J. F. Snowdon, A. J. Waddie (R. A.) and K. J. Symington (Ph. D. student).

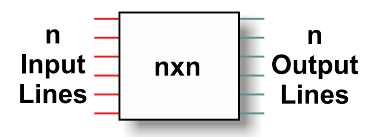
Project funded by EPSRC "Optoelectronic Switch Controller for Telecommunications" grant.

The Assignment Problem

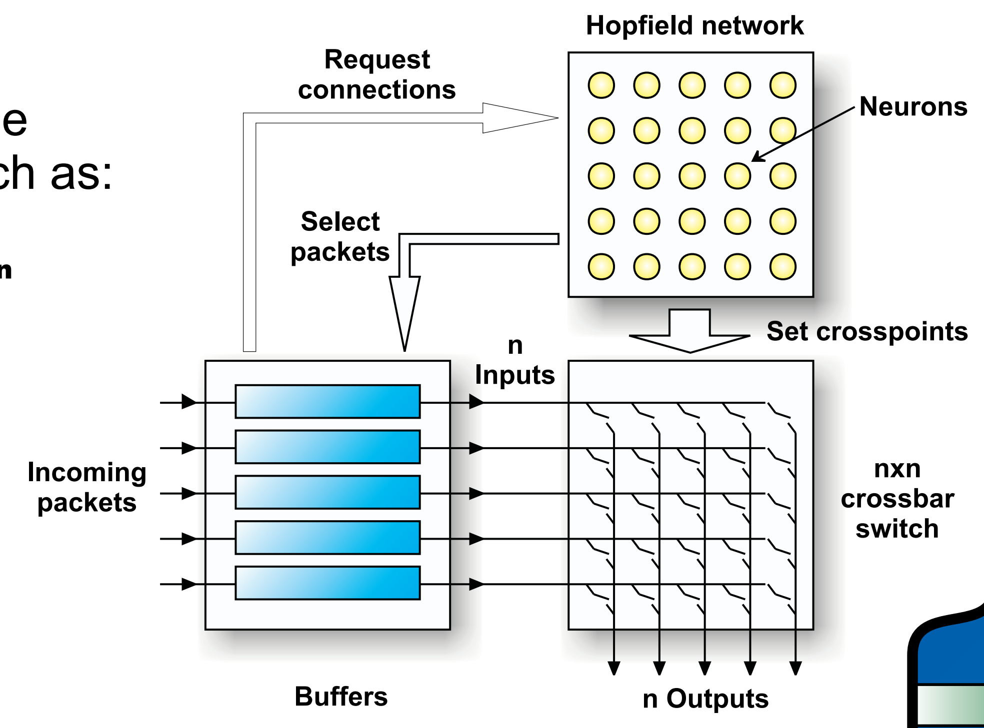
The assignment problem is essentially task allocation optimisation amongst all available resources to maximise throughput. This problem can be found in situations such as:

- Network service management.
- Distributed computer systems.
- Work management systems.
- General scheduling, control or resource allocation.

Schematic Representation

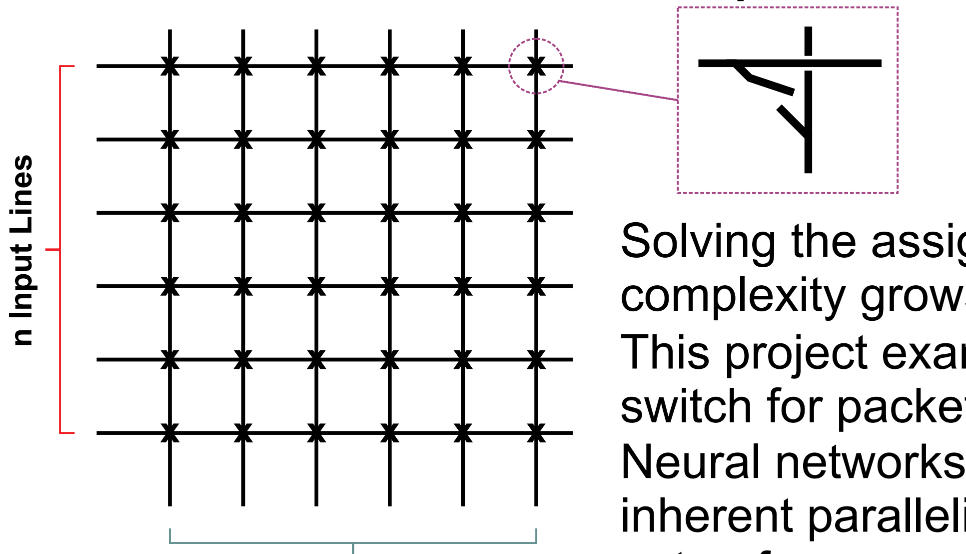


Neural Network Crossbar Switch Controller



Sample nxn Crossbar Switch

Crosspoint Switch



Solving the assignment problem is computationally intensive and complexity grows exponentially with problem size.

This project examines specifically the assignment problem in a crossbar switch for packet routing: maximising throughput and minimising delay. Neural networks are capable of solving the assignment problem. Their inherent parallelism and mode of operation allows them easily to outperform any other known method at higher orders.

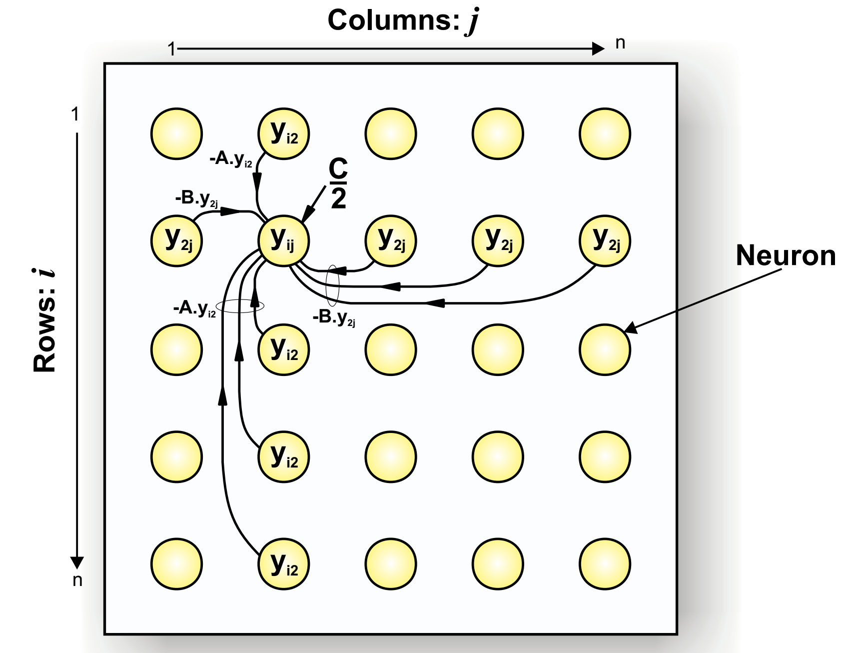
Modified Hopfield Neural Network

The key to utilising the parallelism of a neural network is matching the network as closely as possible to the problem by altering the updating rule.

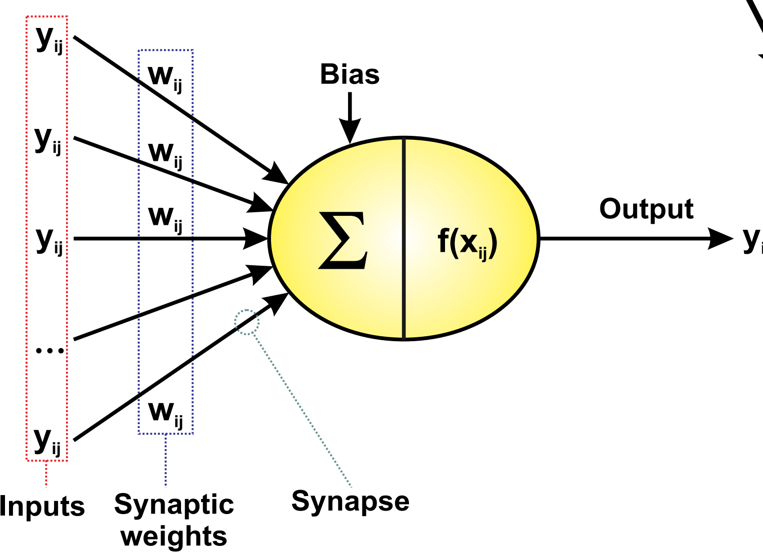
The updating rule determines the next value a neuron will take based on the previous outputs of other neurons:

$$x_{ij}(t)=x_{ij}(t-1)+\Delta t\left(-ax_{ij}-A\sum_{k\neq j}^{n} y_{ik}-B\sum_{k\neq i}^{n} y_{kj}+\frac{C}{2}\right)$$

Modified Hopfield Neural Network Interconnection



Neural Processing Element (Neuron)

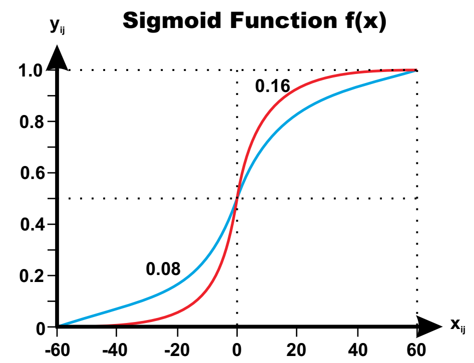


where:

x_{ij}: Summation of all the inputs to the neuron referenced by ij: including the bias.

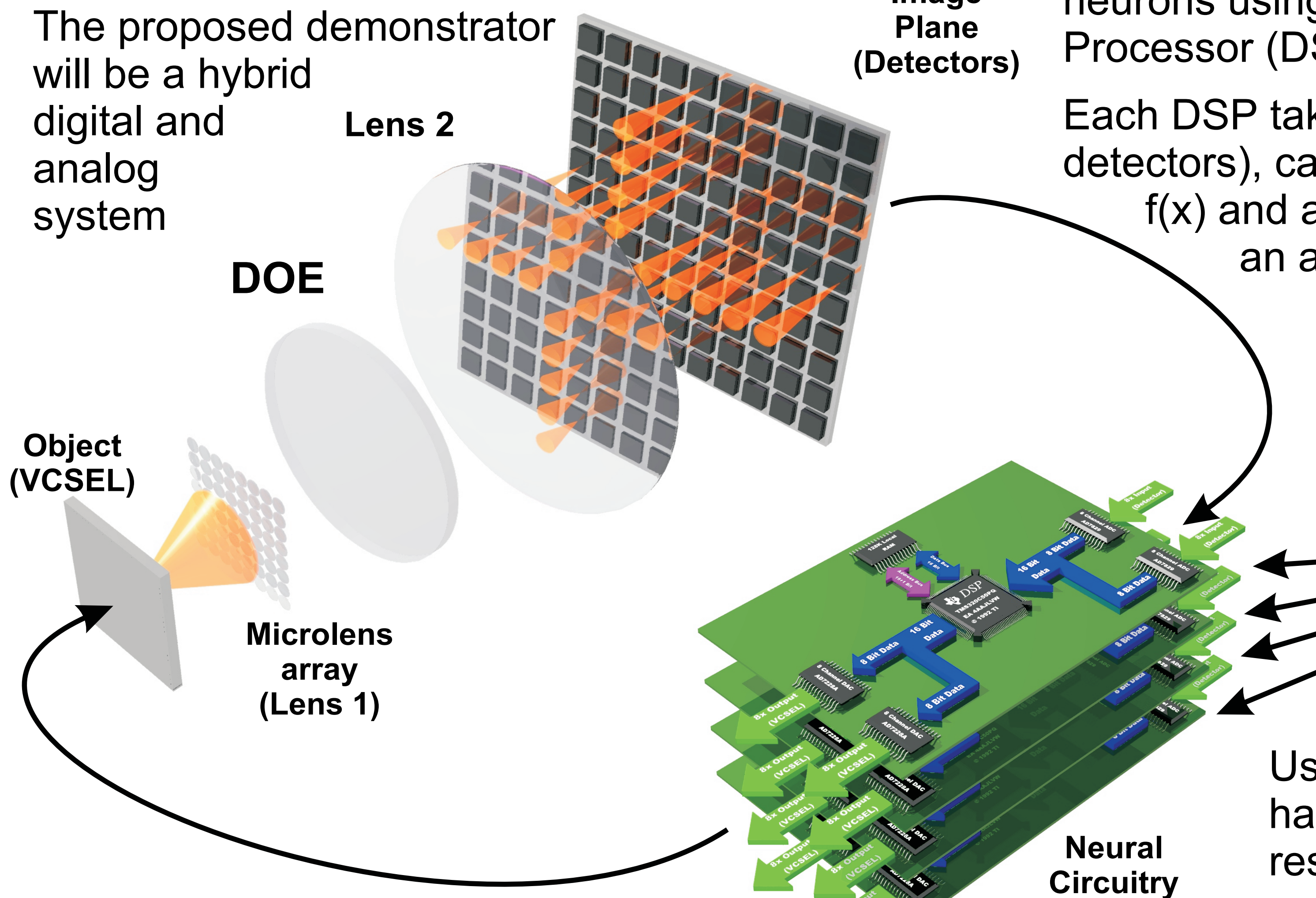
y_{ij}: the output of neuron ij.

A, B and C: Optimisation parameters.



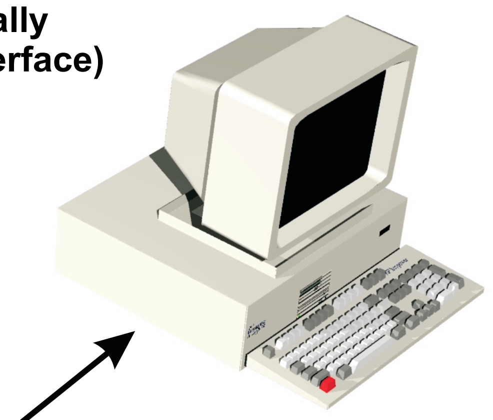
System Implementation

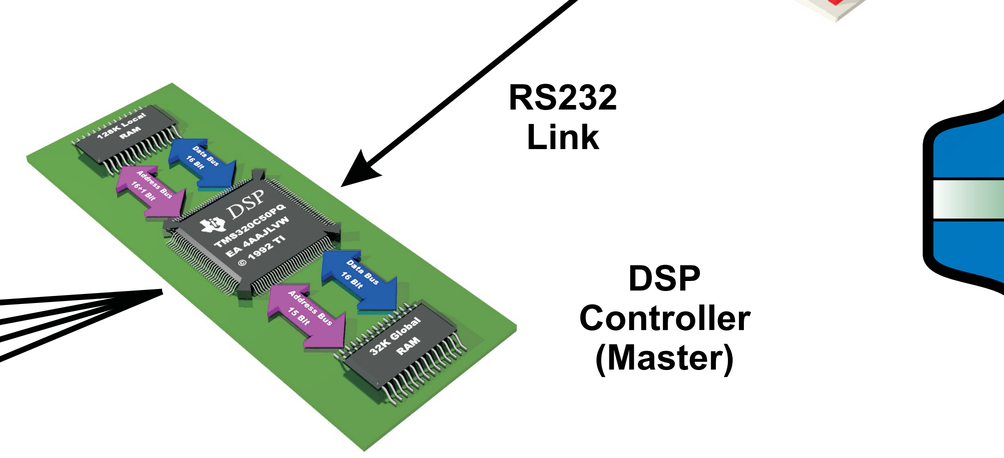
The proposed demonstrator will be a hybrid digital and analog system



This demonstrator will implement neurons using a Digital Signal Processor (DSP): one DSP for 16 neurons.

Each DSP takes 16 analog inputs (from the detectors), calculates the activation function f(x) and adjusts the associated VCSEL to an appropriate analog output level.



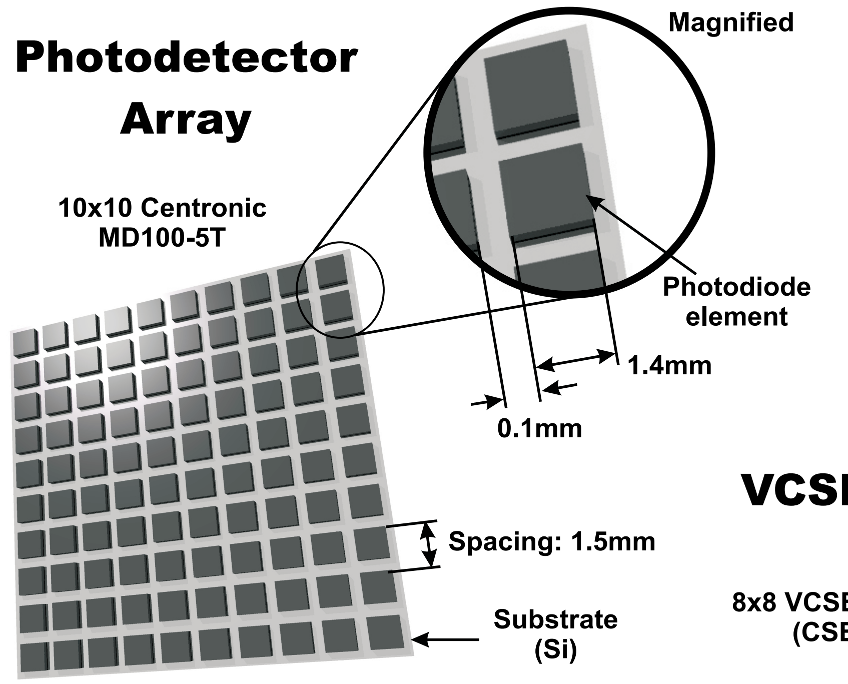


Using DSPs as neurons gives increased flexibility over any hardwired implementation allowing exploration of network response, network configuration and fault tolerance.

The master DSP oversees the DSP neural network and can be used to log its progress or check for convergence.

The Diffractive Optic Element (DOE) performs interconnection by diffracting light to target detectors.

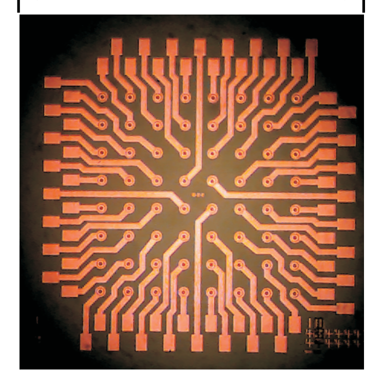
Optical Input/Output

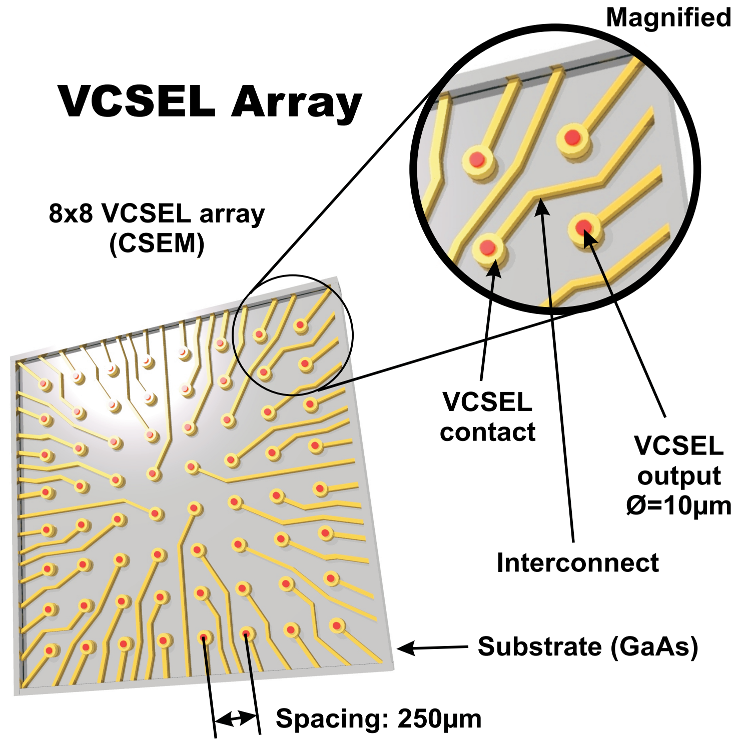


The photodetector array has a typical response time of ~26ns. Only the central 8x8 elements are actually used.

The VCSEL (Vertical Cavity Surface Emitting Laser) is considerably faster with an turn on delay of just 1.6ns.

VCSEL array photograph





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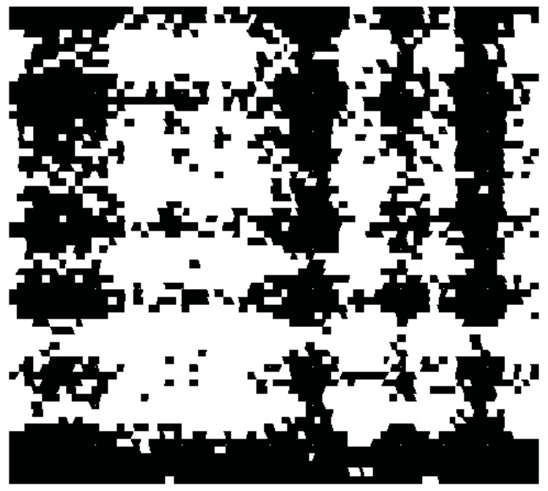
15th February 1999

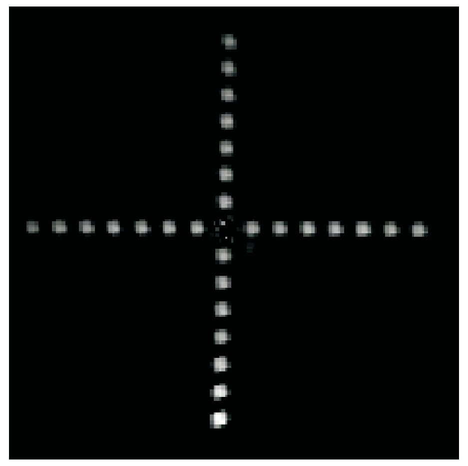
Diffractive Optic Element (DOE) for Hopfield Neural Network

The neural network requires a highly uniform pattern only attainable by using a low-efficiency binary element. Additionally the large period of the detector array forces the DOE to have a small (~80µm) period limiting the number of pixels available to optimise the grating.

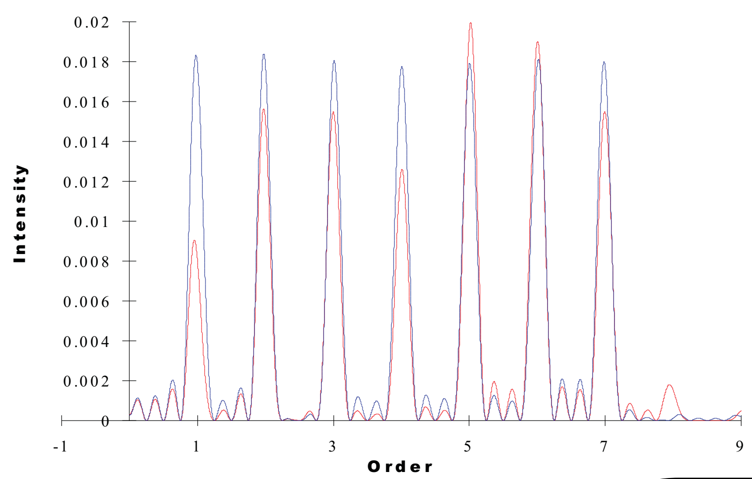
DOE Pattern



DOE Output

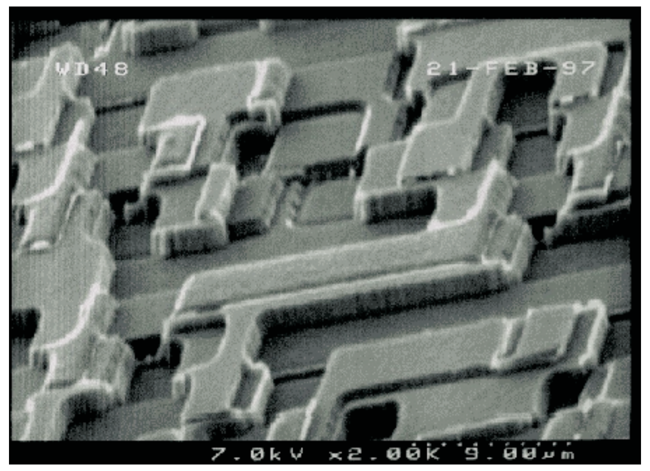


Graph of Intensity versus Order

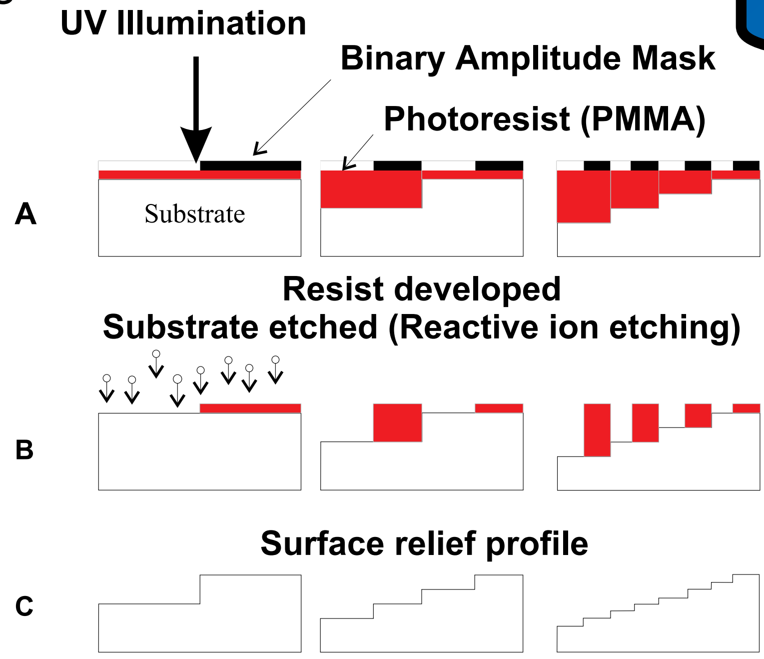


Phase-only DOEs are created by selectively etching fused silica to form phase profiles which have been optimised to produce the desired intensity patterns in the far-field of a Fourier lens. Elements with efficiencies of >70% and non-uniformities of <3% are routinely produced by the Diffractive Optics Group at Heriot-Watt University. These elements are used as array generators and interconnection elements as well as more complex beam shaping elements for laser material processing.

Sample DOE

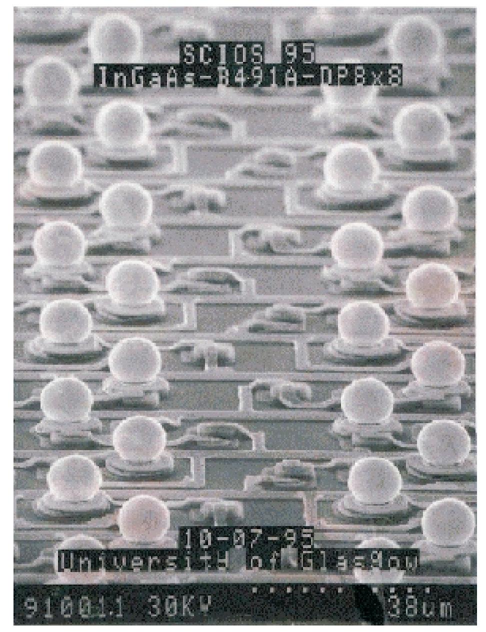


DOE Fabrication Process

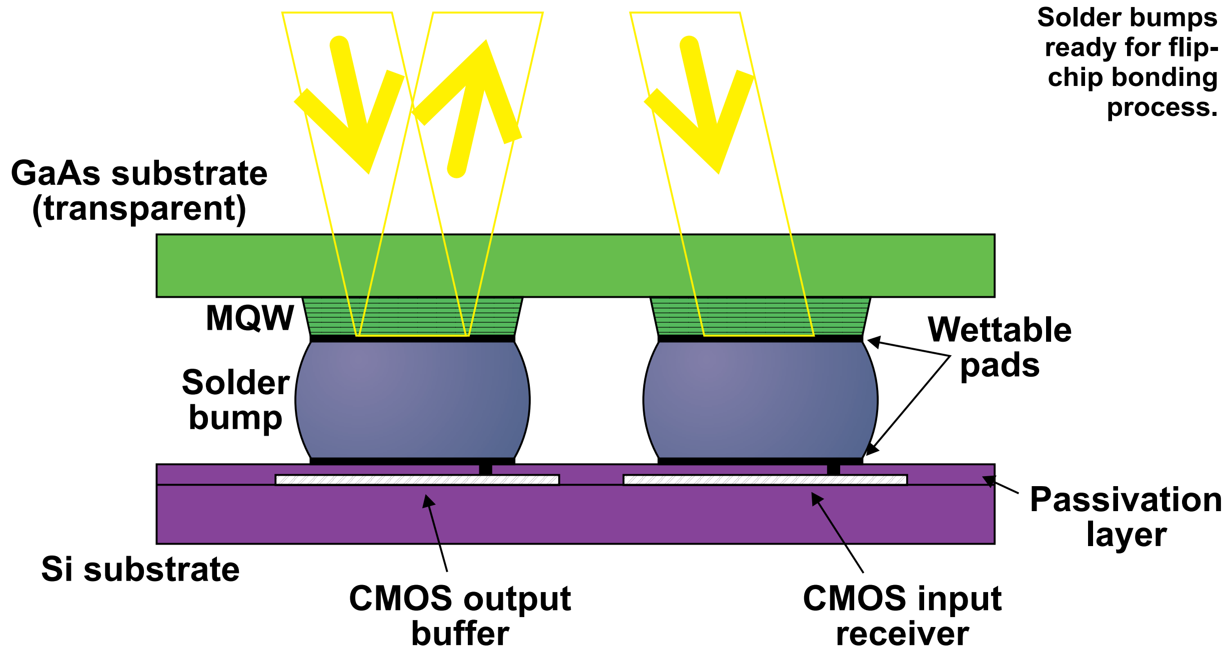


Smart-Pixels

Solder-bumps facilitate the combination of conventional Si-based electronics with optoelectronic components using a process called flip-chip bonding. This hybrid technology allows processing planes of arbitrary functional complexity to be created.



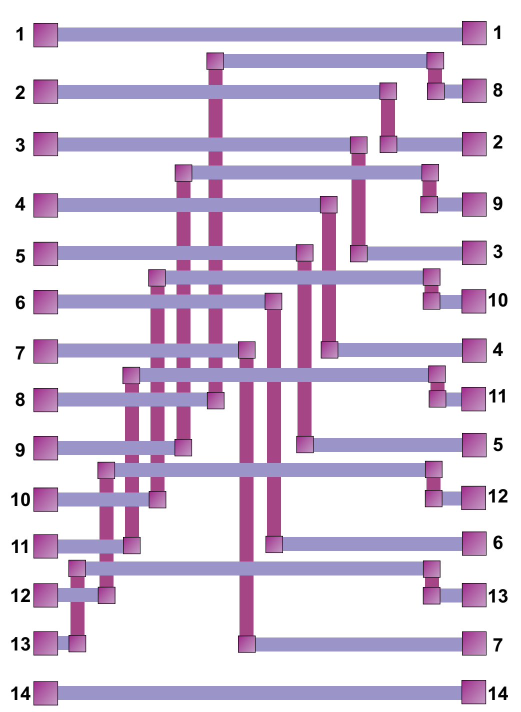
Solder bumps ready for flip-chip bonding process.



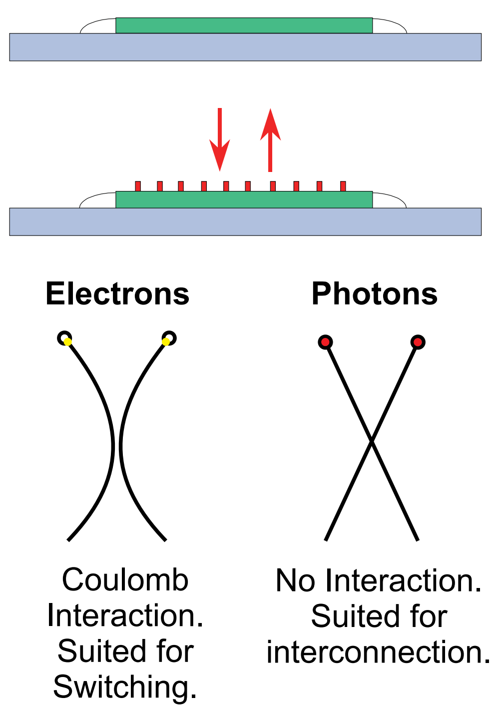
Why Use Free-Space Optics?

Neural networks use simple processing elements where communication is an integral part of their design. Electronics has difficulty implementing scalable non-local interconnects whereas light is non-interacting in free space and therefore the interconnects can effectively cross each other.

2D Interconnect
(Designed for Bitonic sorter)



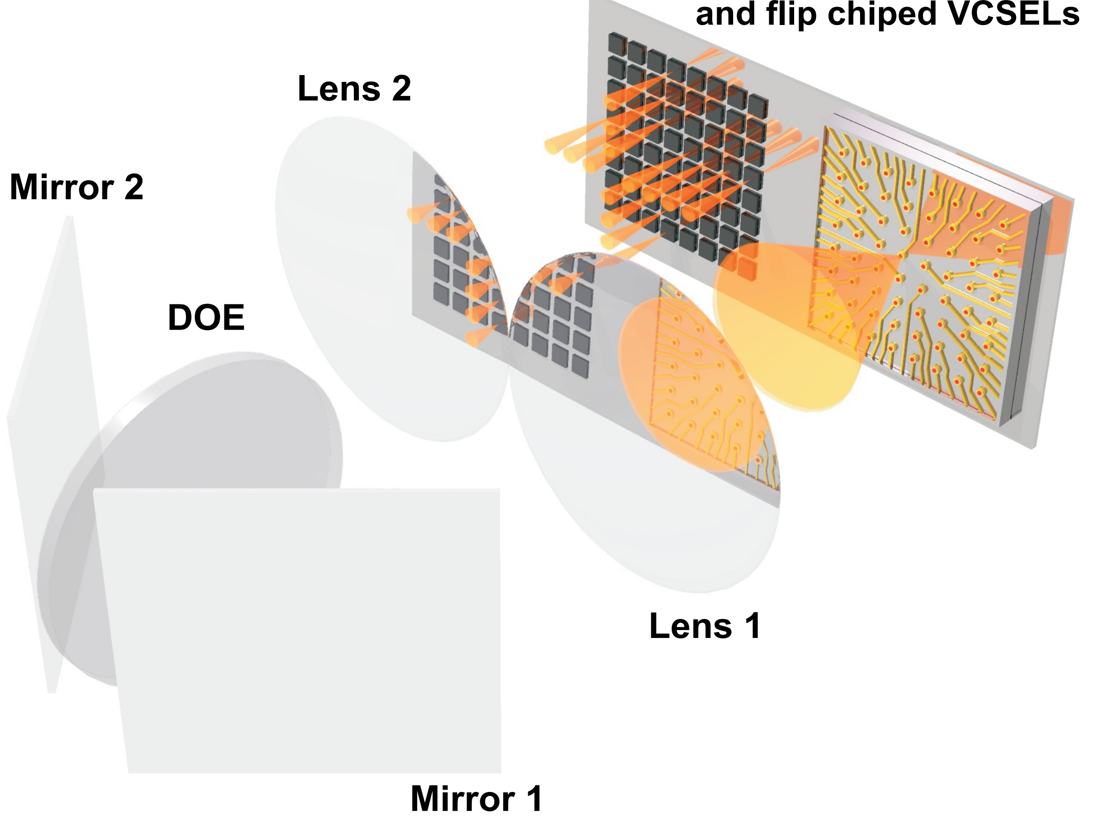
Free-Space Optics



Future Directions

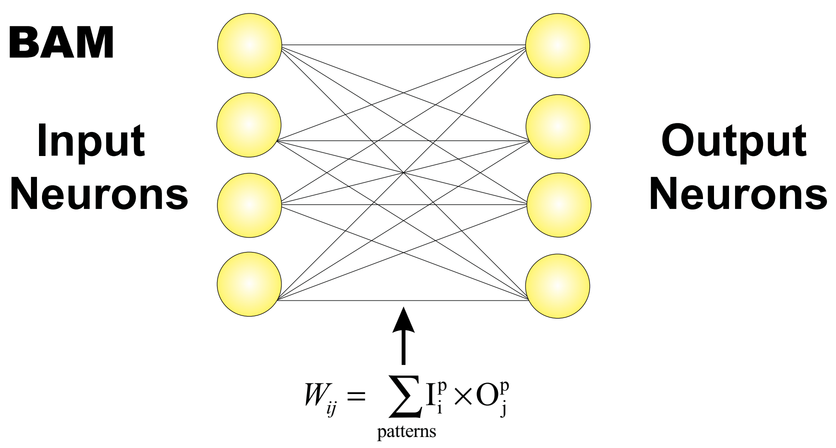
Using 'Flip-Chip' bonding it would be possible to integrate both VCSEL and Detector arrays. This would ultimately allow the creation of a Folded System.

Folded System



Another alternative is to attempt implementation of an Optoelectronic Bidirectional Associative Memory (OBAM).

BAM

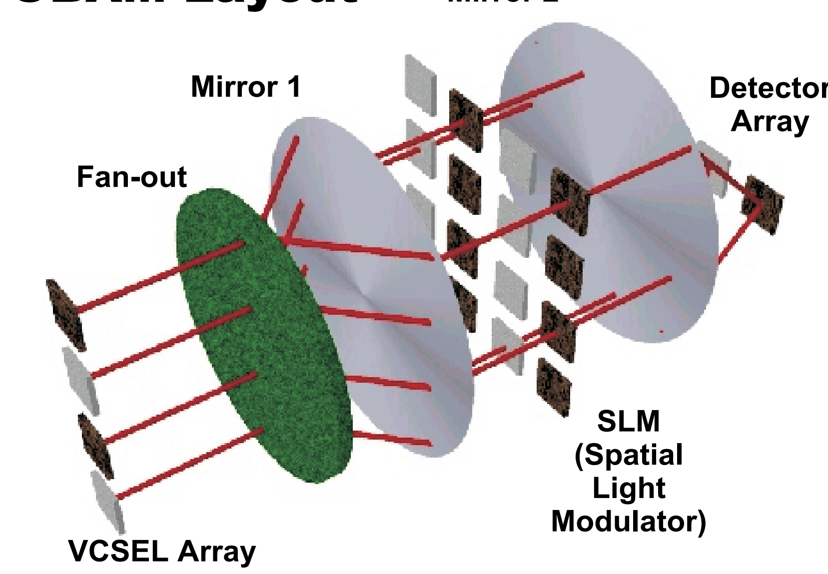


$$W_{ij} = \sum_{\text{patterns}} I_i^p \times O_j^p$$

The BAM has weighted interconnects between the input and output layers but not within the layers. The weighted interconnects are defined by the input and associated output patterns the network is to learn.

The bipolar neurons limit the total number of weight values required to implement the BAM to 2P+1 where P is the number of input/output sets the network is to learn.

OBAM Layout



10 Input - 10 Output OBAM