An Optoelectronic Neural Network Scheduler: Implementation and Operation

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Technical Areas: *Optoelectronics; Neural Networks; Optical Interconnections; Telecommunications Switching*

1. Introduction

The Hopfield neural network[1] is composed of an array of thresholding processing elements, called neurons, and inhibitory interconnections between these neurons. The equations governing the dynamic behaviour of this network are,

$$\frac{dx_i}{dt} = I_i\left[-\lambda x_i - \sum_{j=0}^{N-1} W_{ij} y_j + t_i\right] ,$$

$$y_i = o_{\min} + \frac{o_{\max} - o_{\min}}{1 + \exp(\beta x_i)}$$

where x_i is the state of the i-th neuron, y_i is its output and t is the threshold or bias for the neuron. If a particular neuron is to be entered into the competition between neurons during the current network cycle then I_i is equal to 1 otherwise it equals 0. The overall effect of the inhibitory interconnections (Wij) is to permit only a limited subset of the neurons in the network to achieve an "on" state during any particular operating cycle. By careful selection of the inhibitory interconnection pattern the network can be made to optimise some arbitrary function[2]. In the specific case presented in this paper the inhibitory interconnections are designed to make the network optimise the number of packets which can be switched through a standard crossbar switch during one cycle.

The optoelectronic scheduler for a packet switch described previously[3] successfully demonstrated the validity of the Hopfield approach to this problem. However, the system itself was physically large as well as requiring constant observation to ensure that the diverse electronic and optical components remained operational and in alignment. The next-generation demonstrator has been designed to facilitate "*hands-off*" operation of the demonstrator by using an optomechanical baseplate in conjunction with both off-the-shelf and custom designed optical, electronic and optoelectronic subsystems. In this paper we shall report on the progress of each of these elements of the system as well as investigating the limitations on the scalability of the system imposed by the different subsystems.

2. Optical Subsystems

The optical subsystem of the neural network hardware implements the inhibitory interconnections between the neurons by means of a diffractive optical element (DOE) and lens combination. This approach allows maximum flexibility of interconnection pattern as the interconnection pattern can be changed by placing a different DOE in the system. The neurons themselves are implemented electronically using a number of Digital Signal Processors and will be discussed in Section 3. The electronic-optic conversion is performed by a 2D (8x8) array of Vertical Cavity Surface Emitting Lasers, operating at λ=960nm, and a 2D (8x8) array of Si photodetectors is used to convert the optical signals back to electronic signals. The entire optical subsystem, which includes the optomechanic and optoelectronic subsystems, is shown in Figure 1 with the optical signals passing from right to left. The lens (effective focal length = 10cm) used in this assembly was chosen to provide the necessary x6 magnification to match the VCSEL pitch (250μm) to the photodetector pitch (1.5mm). The optomechanical slotted baseplate design simplifies the alignment of the VCSEL array with the photodetector array as well as allowing the relative longitudinal positions of the lens and DOE to be altered without changing their transverse positions.

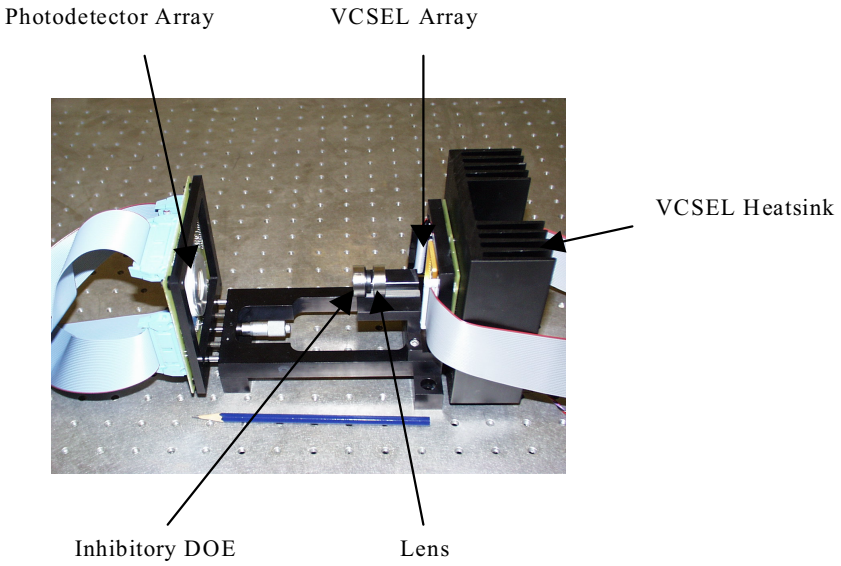

Figure 1 : Optomechanical Baseplate and Optical Subsystem for Optoelectronic Hopfield Network Scheduler

The diffractive optical element was designed using a combination of an iterative Fourier transform algorithm[4] (IFTA) and a closed-form trapezoidal algorithm[5]. In general, these standard design methods allow the creation of DOEs with efficiencies of > 70% and reconstruction errors of < 1%. However, due to the restrictions placed upon the DOE period by the optical system described above, a reduction in the overall efficiency of the DOE to 50% was required to ensure that the reconstruction error was of an acceptable level. The period of the DOE is given by,

$$T = \frac{nf\lambda}{s}$$

where n is the number of orders between co-linear "on" diffraction orders, f and λ are the focal length and wavelength respectively and s is the separation between "on" diffraction orders. Figure 2 shows the output from two different inhibition DOEs, the first was designed with the co-linear spacing between the "on" diffraction orders set at one diffraction order and the second with the co-linear spacing set to two diffraction orders.

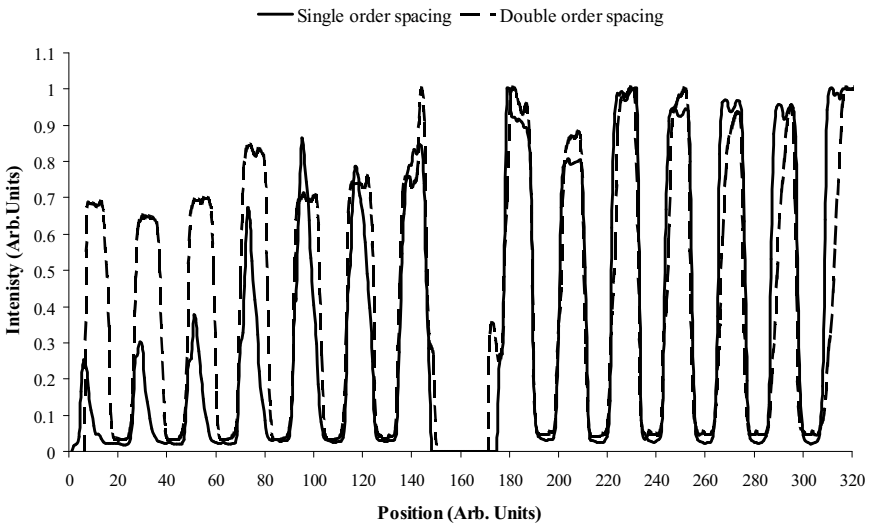

Figure 2 : Cross section through inhibition interconnection DOE

It can be seen from Figure 2 that the larger period produced by the double order spacing has improved the overall uniformity of the element. This improvement in final uniformity is due to the larger minimum feature size of the double order spacing element and the commensurate improvement in the photolithographic transfer of the phase profile onto the glass substrate.

3. Electronic Subsystems

The electronic subsystem of the neural demonstrator consists of five stages, each performing a specific task as shown in Figure 3.

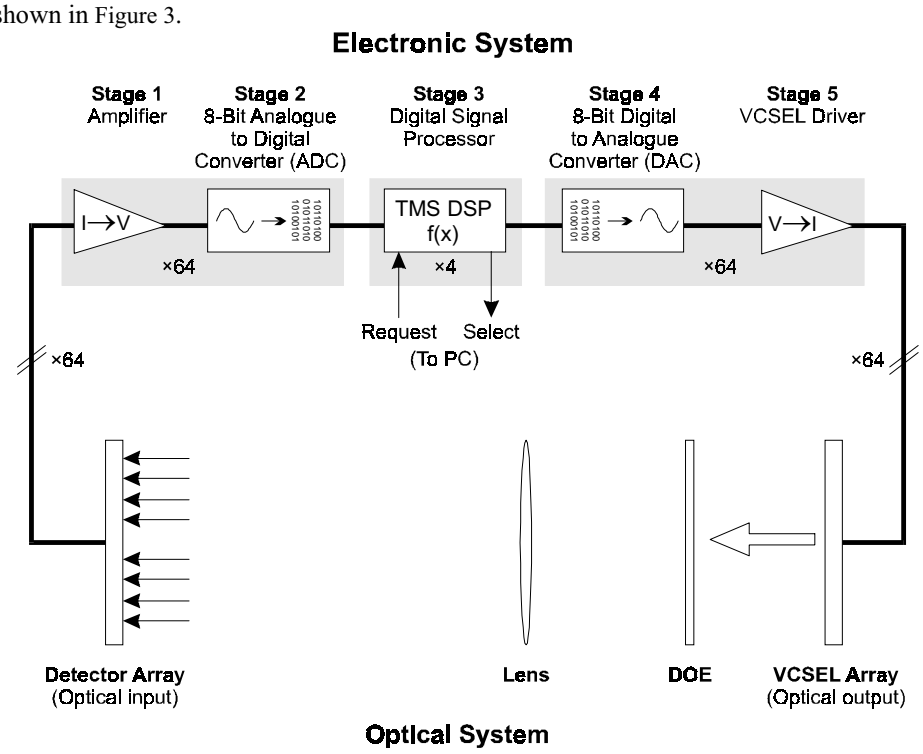

Figure 3 : Electronic and Optical subsystem components.

Starting at the optical input there is a detection system that converts the photocurrents generated by the photodetector array in to voltages. These voltages are passed through 8-bit analogue-to-digital converters (ADCs) and the converted signals are time-multiplexed onto the Digital Signal Processors, which comprise the next stage. This stage consists of 4 Texas Instruments TMS320C5X DSPs that take the digital information from the ADCs and performs the dynamic update and transfer functions specified earlier. The fourth stage converts the digital values generated by the DSPs back into analogue voltages, using 8-bit digital-to-analogue converters, for delivery to the final stage which is the driver circuitry for the Vertical Cavity Surface Emitting Laser array. The use of off-the-shelf DSPs to implement the neural thresholding functions allows the functionality of the network to be altered and new problems to be tackled with minimal alteration of electronic and optoelectronic hardware. Currently, there are four DSPs operating in a time-multiplexed manner where each DSP handles 16 inputs and 16 outputs in any one network cycle. The DSPs act as slaves to a master CPU, in this case a PC, which can be used to reprogram the DSPs.

Two different VCSEL driver circuits were designed, the first using discrete digital components to provide the necessary drive current and the second a custom-designed application specific integrated circuit (ASIC) fabricated through the MOSIS brokerage service. Figure 4 shows the photodetector driver circuit output voltage swing generated by the far-field output of the inhibitory interconnection DOE under illumination from a single VCSEL modulated at 5kHz.

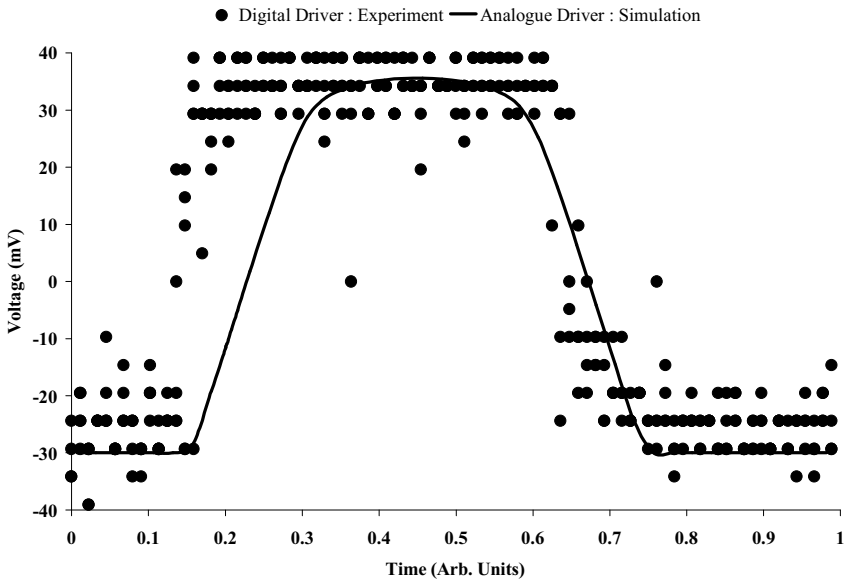

Figure 4: Output Voltage generated by photodetector driver circuit under illumination from modulated VCSEL output.

The modulation frequency is significantly below the theoretical maximum modulation frequency of both driver circuits (100 MHz for the digital driver and 10 MHz for the analogue driver) and it was chosen to allow the data acquisition card used in the experimental system to accurately measure the voltage. The experimental digital driver was modulated using a TTL (0-5V) square wave and the simulated analogue driver was driven using a 1V-2V sinusoidal wave, both being sufficient to produce enough current to switch the VCSEL between no optical output and an optical output of ~1mW. The total amount of optical power incident upon a single photodetector from one VCSEL has been calculated to be,

$$P_{\text{sin}\,gle} = \eta_{bulk\_optics} \frac{\eta_{DOE}}{4(N-1)} \times P_{VCSEL}$$

which for the demonstrator hardware presented in this paper (N=8, η_{bulk_optics} =0.95, η_{DOE} =0.5 and P_{VCSEL}=1mW) is equal to ~17μW. The observed voltage swing of 60mV (corresponding to an optoelectronic amplification of 3500) for a single incident beam implies that the total voltage swing for a photodectector with the maximum number (14) of optical inputs incident upon it will be ~1V.
Figure 5 shows the fabricated analogue VCSEL driver, which is currently being tested and will replace the digital driver circuit in the completed demonstrator system.

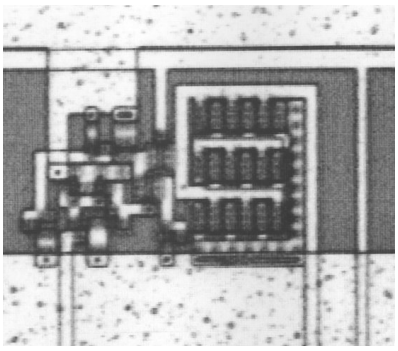

Figure 5 : Micrograph of analogue VCSEL driver circuit designed using a 2-poly 2-metal 1.5μm process.

4. Scalability of the Optoelectronic Hopfield Network

In principle, the Hopfield network architecture discussed in this paper is highly scalable with the maximum size of network being set, at present, by the size of available 2D arrays of VCSELs and photodetectors. However, in practice a more fundamental limitation on the maximum size of network which can be realised is imposed by the non-uniformity of the diffractive optical element. This quantity, also known as the reconstruction error, is a measure of the divergence of the observed far-field diffraction pattern from the ideal pattern used in the optimisation of the phase profile. This is expressed mathematically as,

$$\Delta r = \max_{m,n \in M} 1 - \frac{I_{mn}^{\text{observed}}}{I_{mn}^{\text{target}}}$$

where M is the set of diffraction orders used to specify the far-field output of the phase element. Typically, the non-uniformity of binary (2 level) phase elements is of the order of 0.1% after the design process and 1-2% after fabrication. The observed increase in non-uniformity after fabrication is due to inaccuracies in the etching of the glass substrate as well as poor photolithographic transfer of fine (high spatial frequency) features from the e-beam written mask to the glass substrate. Figure 6 shows a section of a grating with minimum feature sizes of ~1.5μm which is the limit of the in-house DOE fabrication facilities at Heriot-Watt University. The sharp features of the ideal phase profile have become rounded and some of the finest features have disappeared.

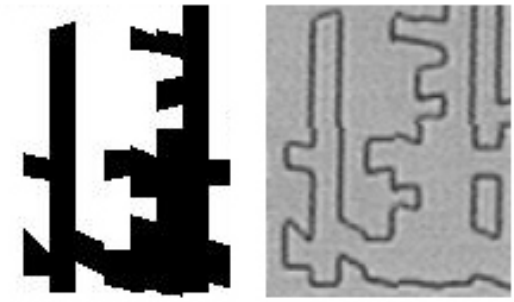

Figure 6 : Section of inhibition pattern DOE showing photolithographic blurring of sharp features.

In order to quantify the effect of DOE non-uniformity on the optoelectronic Hopfield network a simulation of the system was implemented with a non-uniform inhibition interconnection. By varying the total non-uniformity of this interconnection and observing the acceptance ratio, defined here as the proportion of test cycles where the optimal number of data channels are routed through the crossbar switch, an estimate of the limitation on network size due to interconnection non-uniformity can be derived. The optimal number of data channels which can be routed through an NxN crossbar switch is N. Figure 7 shows the variation of acceptance ratio with increasing levels of interconnection non-uniformity for three different Hopfield network sizes. In each case 10000 cycles of the network were analysed and it was observed that when the network was operating correctly, the acceptance ratio was above 99%.

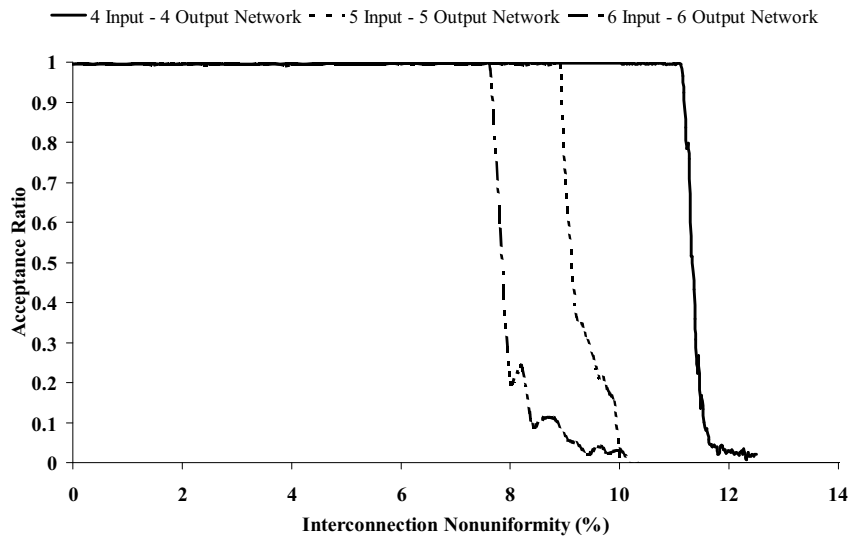

Figure 7 : Variation of Acceptance Ratio with Interconnection Non-uniformity

It can be seen that as the size of the network increases the maximum non-uniformity that can be tolerated decreases. This simulation was repeated for a range of different network sizes and the maximum non-uniformity at which the acceptance ratio begins to decline is plotted in Figure 8.

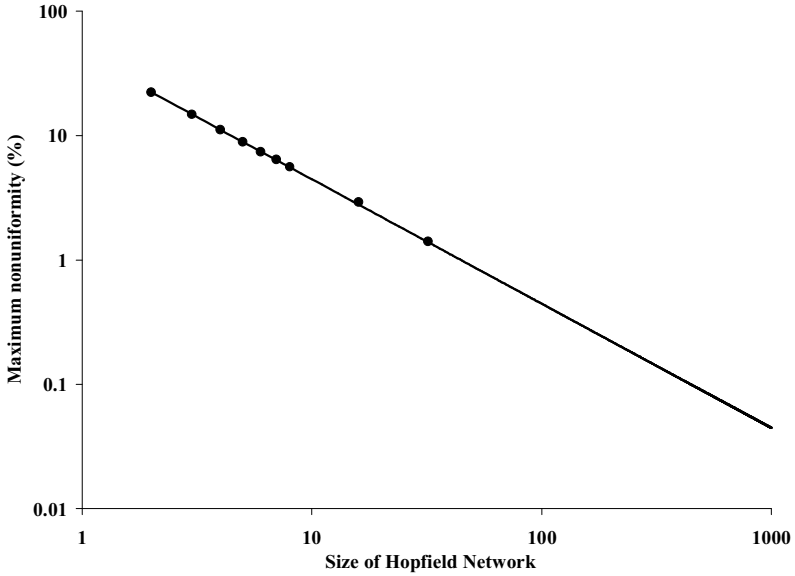

Figure 8 : Maximum Interconnection Non-uniformity

The line in Figure 8 is a fit to the simulated points allowing the trend to be extrapolated to larger networks that cannot be simulated in reasonable time. The maximum interconnection non-uniformity for an NxN Hopfield network is given by,

$$\Delta r_{\max} = \frac{1}{C_1 \times N + C_2}, \text{ where } C_1 = 0.0225 \text{ and } C_2 = -0.000192$$

By assuming that the minimum non-uniformity of any interconnection DOE is 2% and solving the above equation, the maximum size of Hopfield network which can be implemented using the current DOE fabrication technology is 22x22. By changing the optical subsystem to allow a larger DOE period the minimum non-uniformity can be reduced, provided care is taken to remove excessively sharp

features from the phase profile during the design phase. In addition, improvements in the photolithographic techniques used in the fabrication of diffractive optical elements will allow finer features to be resolved which will again reduce the minimum non-uniformity. A combination of these methods will allow the maximum size of Hopfield network to be increased to around 64x64 before unavoidable systemic errors (e.g. in the etch depth) in the fabrication process become significant.

5. Conclusions

We have presented the current state of the next-generation Hopfield neural network demonstrator. The different subsystems have been designed and constructed and have been shown to be operating in the desired manner. Several areas where system performance can be improved have been identified, for example, by using larger order separations and hence larger period DOEs, the effect of DOE fabrication-induced non-uniformity can be reduced, increasing the scalability of the Hopfield neural network architecture. The VCSEL driver circuitry, both digital and analogue, has been shown to operate in the desired manner and, in combination with the photodetector subsystem, to produce a sufficient voltage swing for detection by the digital signal processor neurons.

6. References

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