

An Optoelectronic Neural Network Packet Switch Scheduler

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<http://www.optical-computing.co.uk>

Outline

- The packet switch scheduler - computationally hard, intensive task.
- Simple neural network solution.
- Neural network mapping onto simple optoelectronic system.
- Implementation and results.
- Scalability.
- Active control and optimisation.

The Assignment Problem

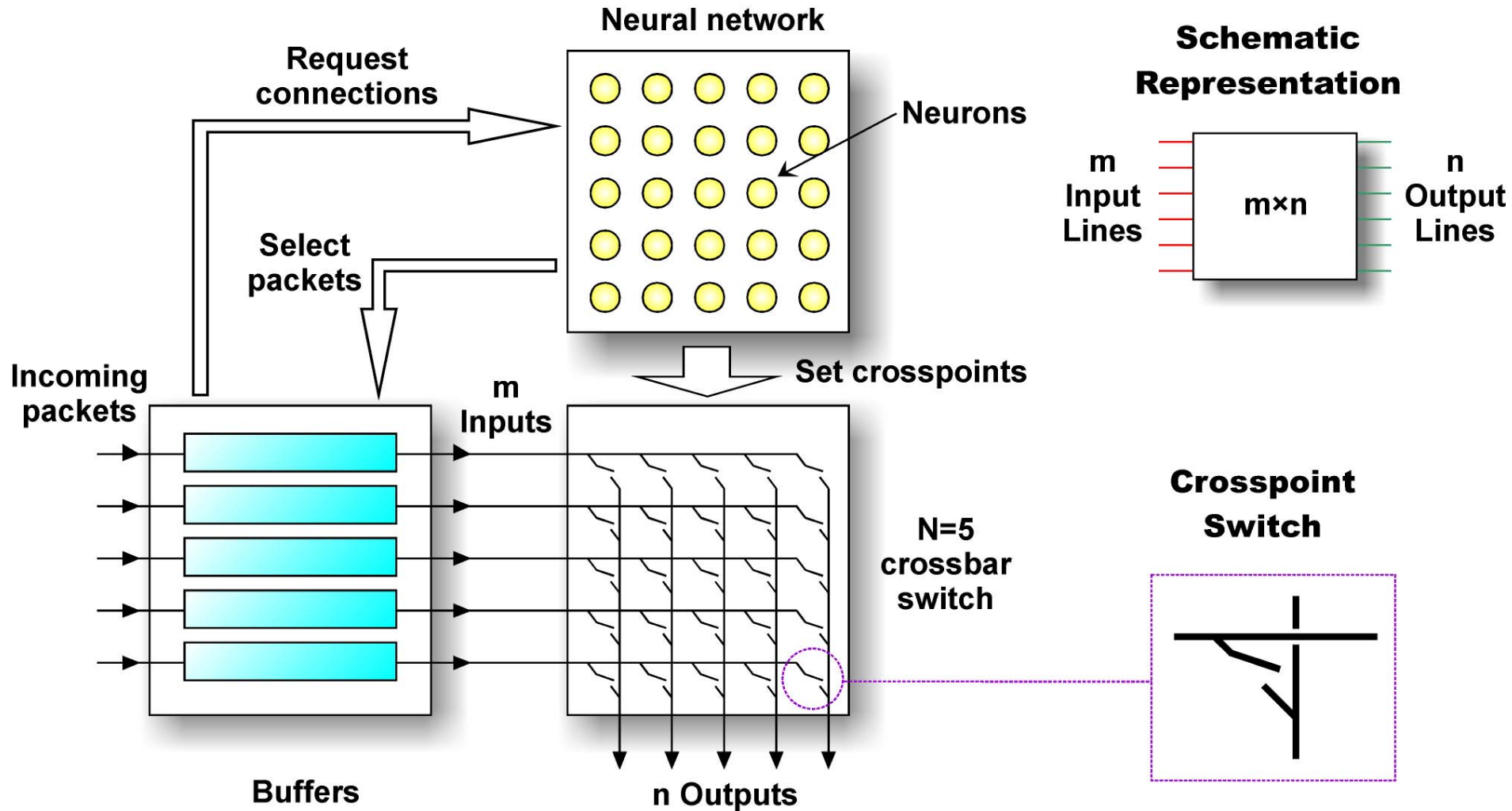
Can be found in situations such as:

- Network service management.
- Distributed computer systems.
- Work management systems.
- General scheduling, control or resource allocation.

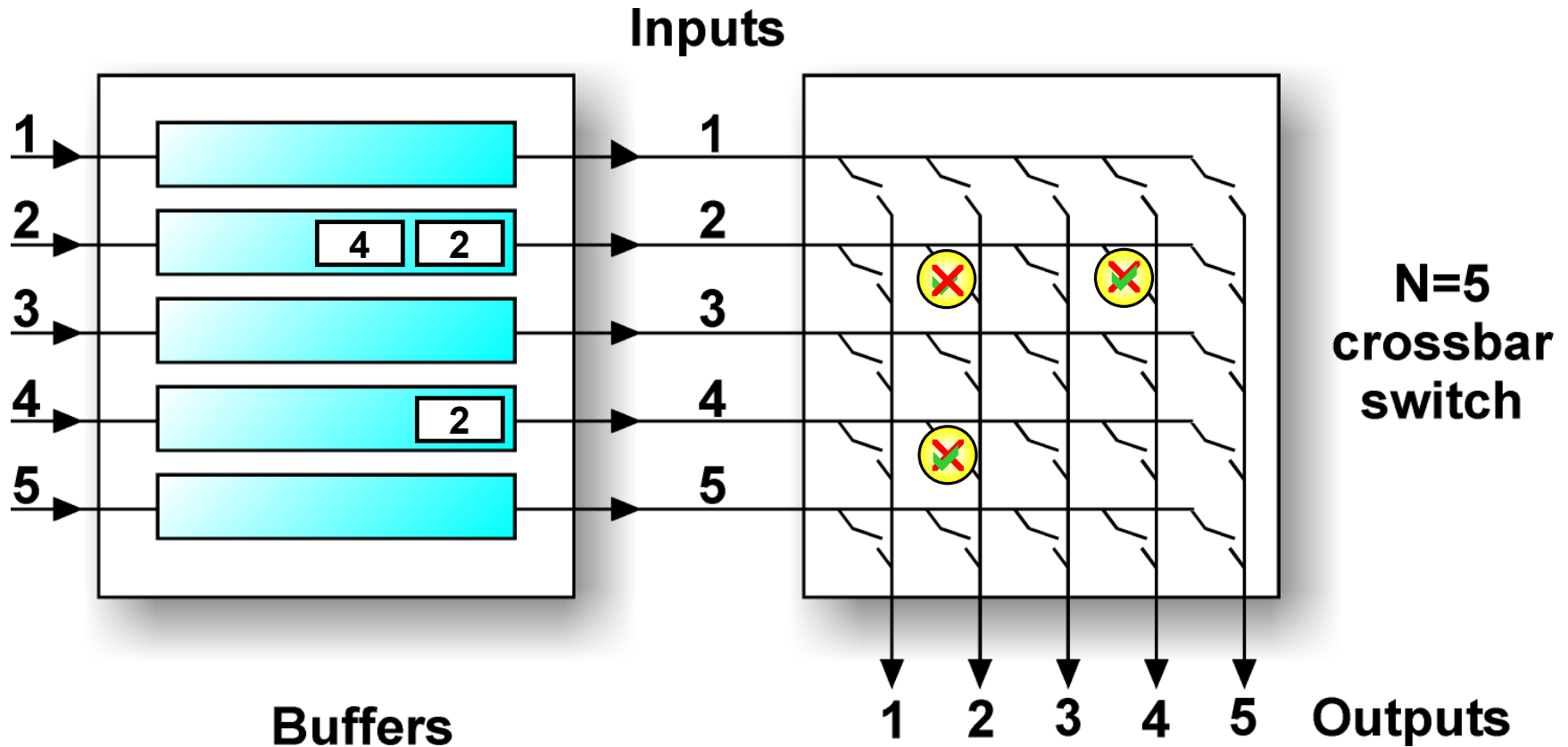
Solution is computationally intensive.

The inherent parallelism of neural networks allows them to outperform any other known method at higher network sizes.

Crossbar Switching

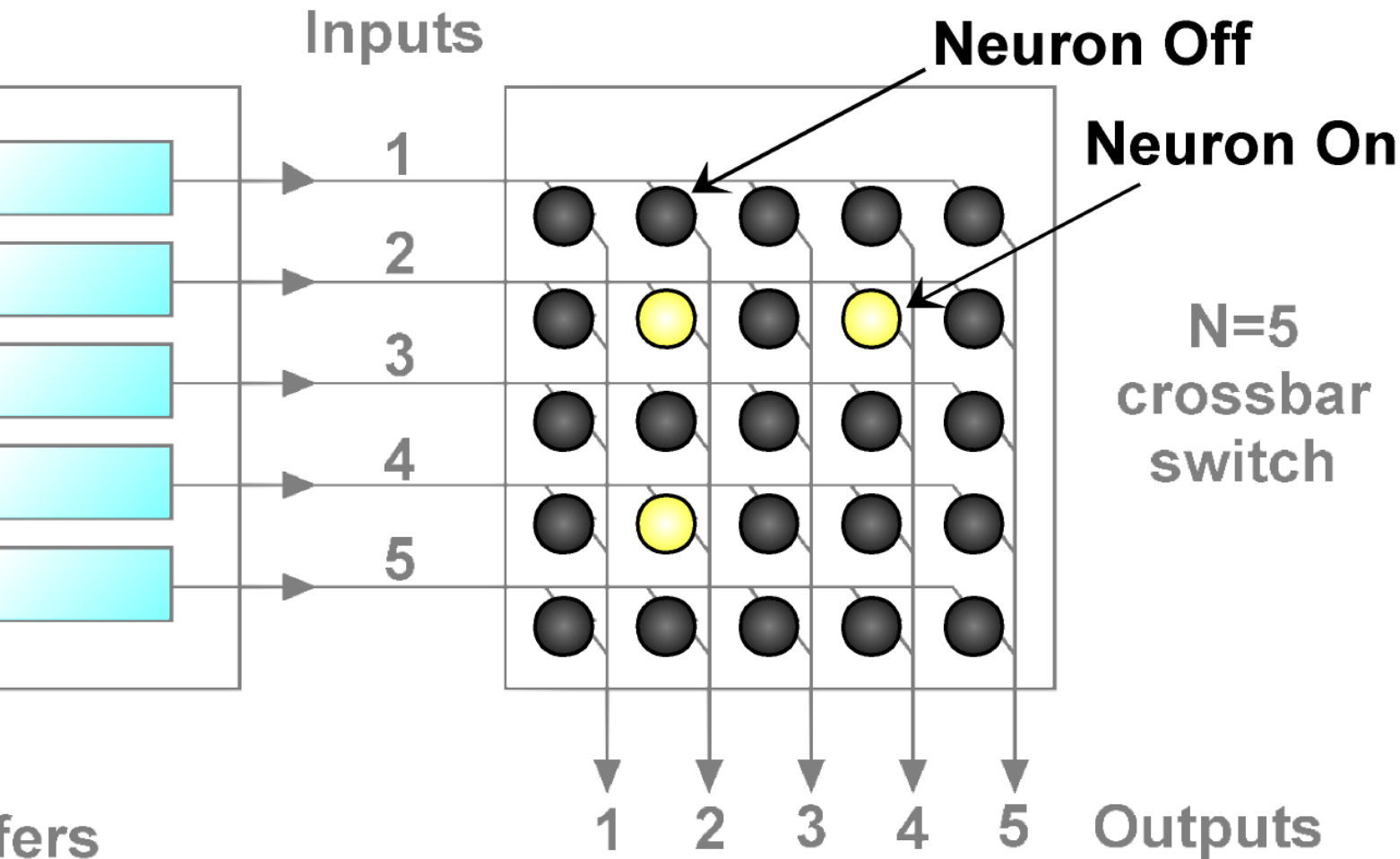


Solution Optimality



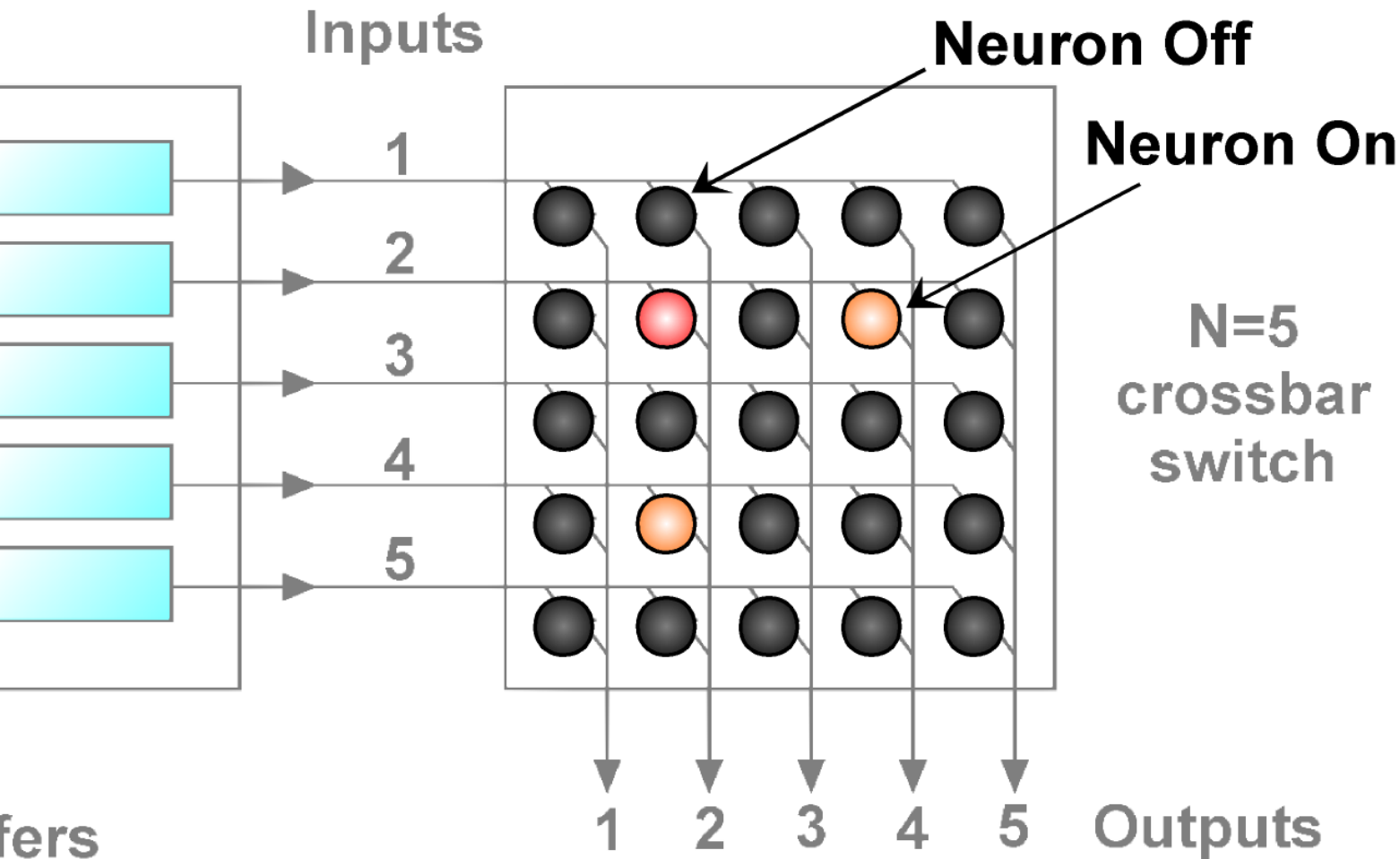
- Routing input 2 to output 2 allows only 1 packet to pass. Solution is sub-optimal.
- Routing input 2 to output 4 and input 4 to output 2 allows 2 packets to pass. Solution is optimal.

Convergence Example



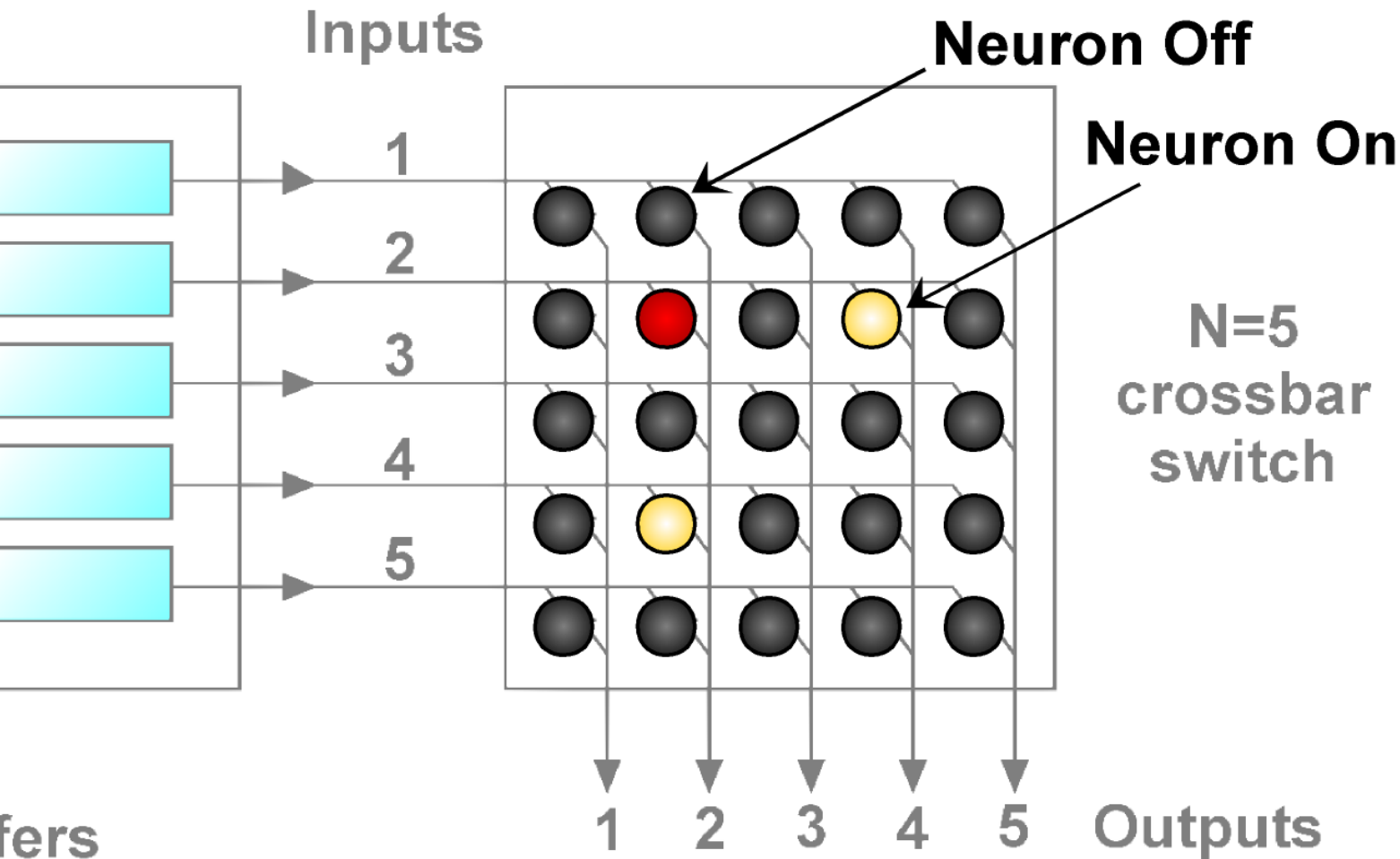
Start state – all requested neurons are on.

Convergence Example



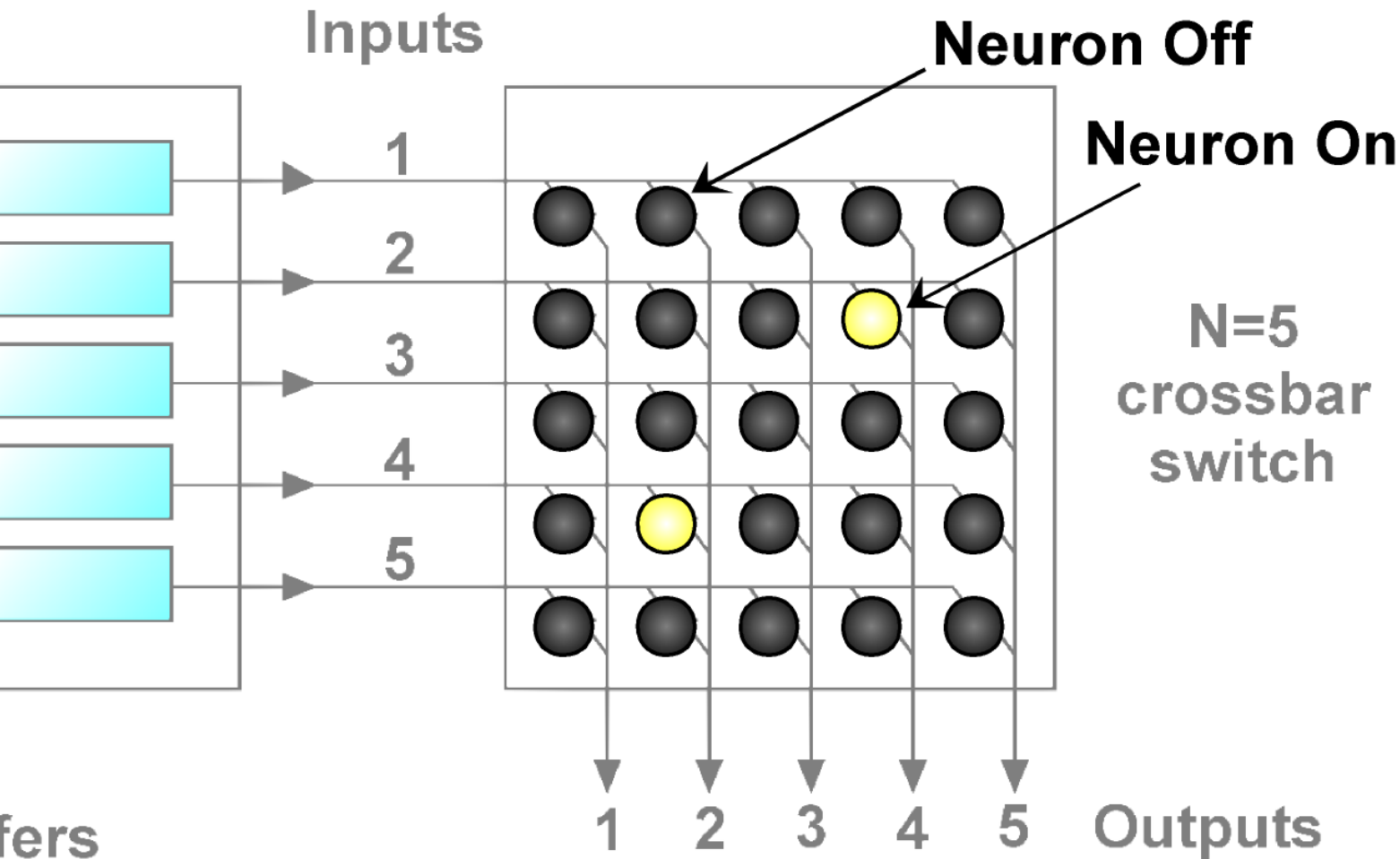
1/3 Evolved: Neurons (2, 4) and (4, 2) are beginning to inhibiting neuron (2, 2).

Convergence Example



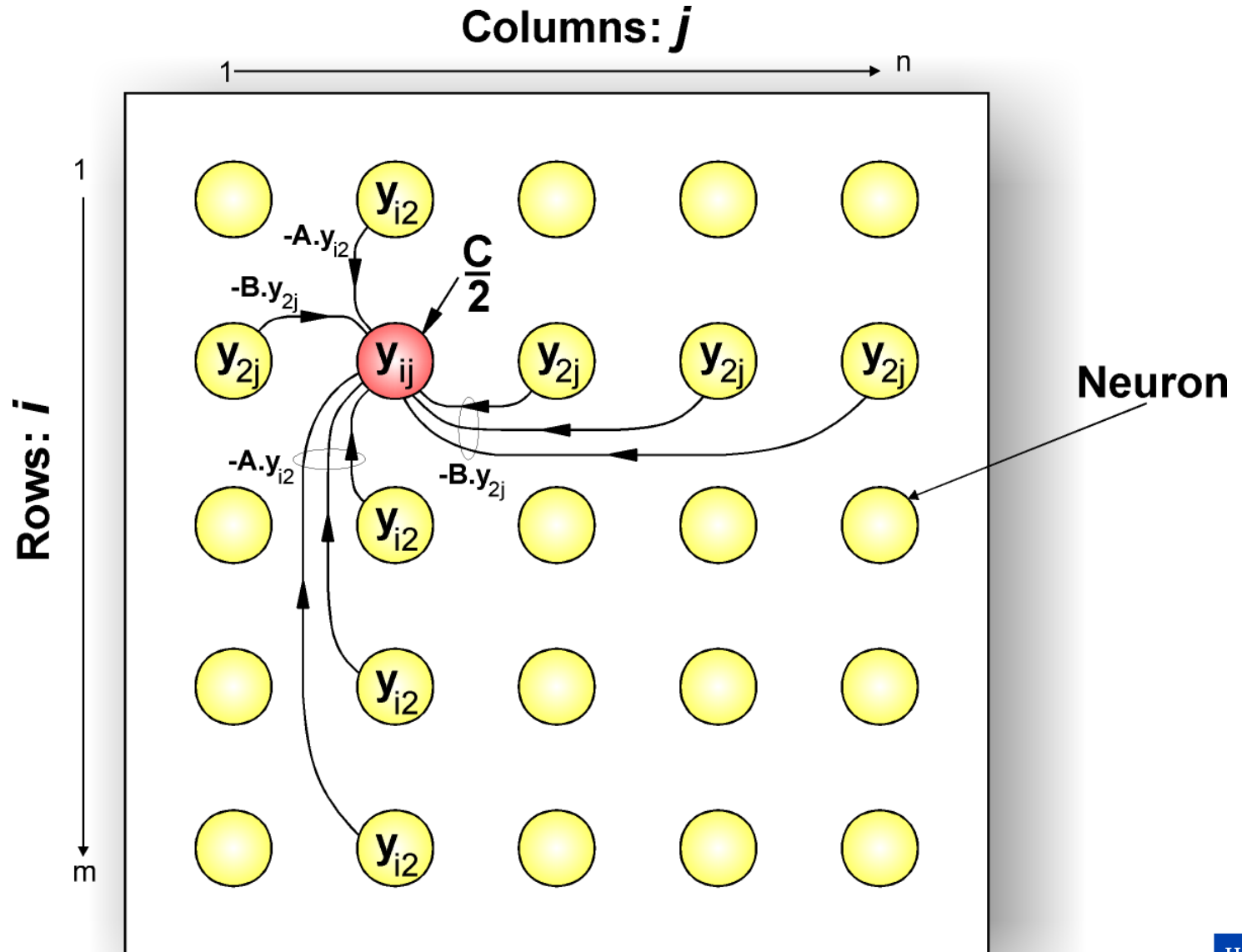
2/3 Evolved: Neuron (2, 2) is nearly off.

Convergence Example



Fully Evolved. Optimal solution reached.

Neural Interconnect



Neural Algorithm

Next state defined by:

$$x_{ij}(t) = x_{ij}(t-1) + \Delta t \left(-A \sum_{k \neq j}^n y_{ik} - B \sum_{k \neq i}^n y_{kj} + \frac{C}{2} \right)$$

x_{ij} : Summation of all the inputs to the neuron referenced by ij : including the bias.

y_{ij} : Output of neuron ij .

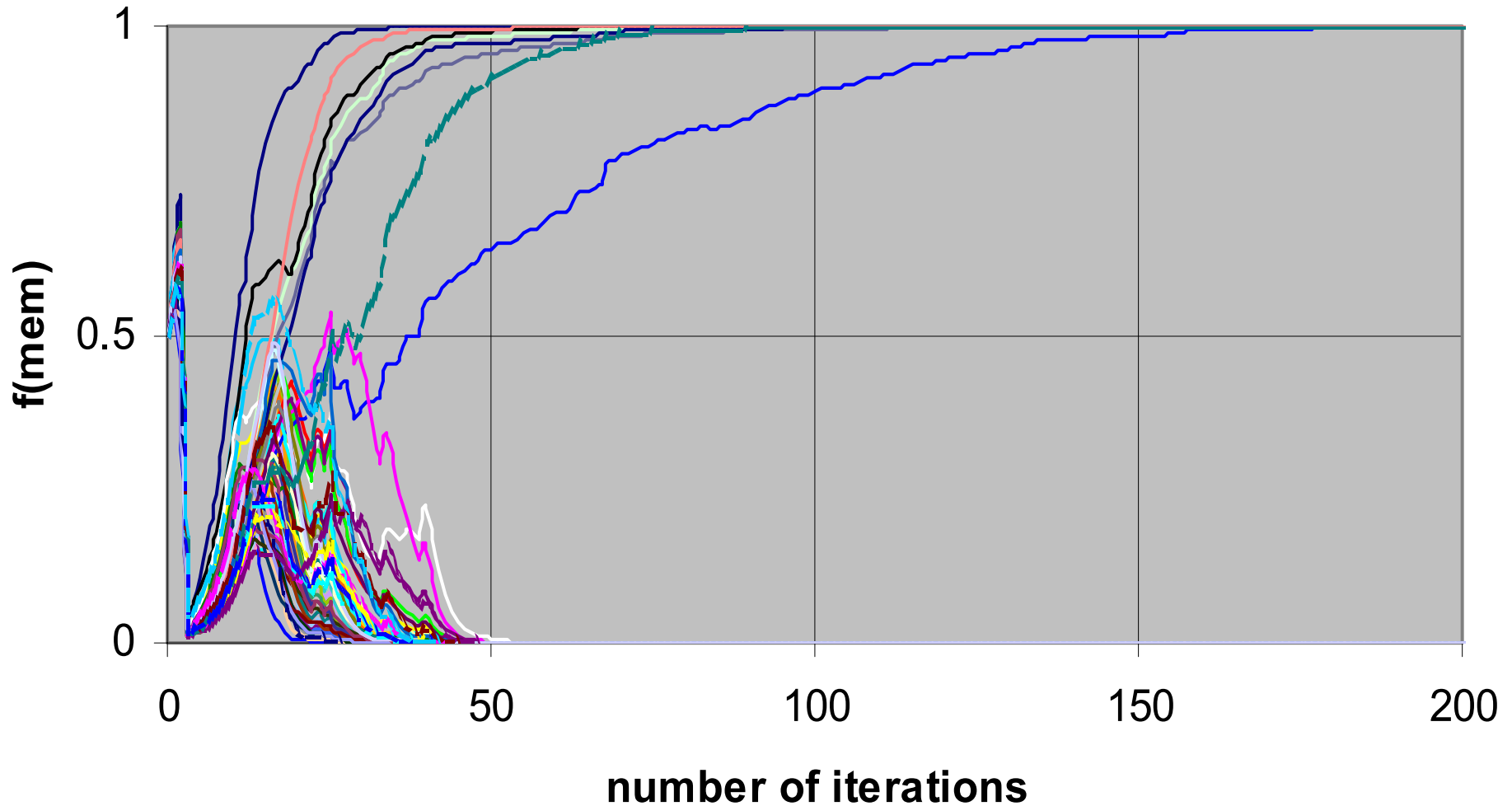
A , B and C : Optimisation parameters.

Neural transfer function:

$$y_{ij} = f(x_{ij}) = \frac{1}{1 + e^{-\beta x_{ij}}}$$

β : Controls gain of neuron.

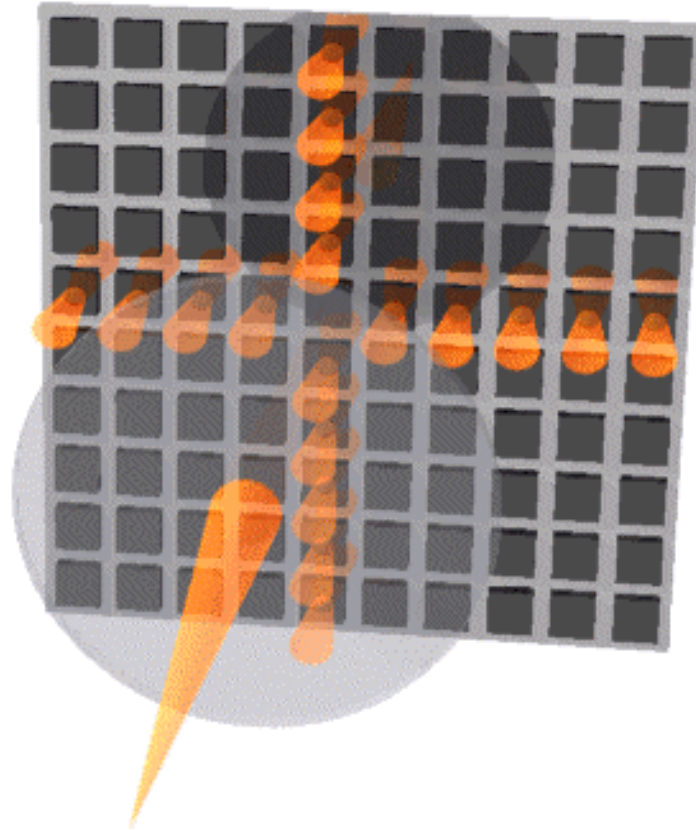
Neuron Evolution



Why Optoelectronics?

- Neural network scalability limited in silicon.
- Free-space optics can be used to perform interconnection.
- Only transfer function $f(x)$ need be performed in silicon.
- Input summation is done in an inherently analogue manner.
- Noise added naturally.

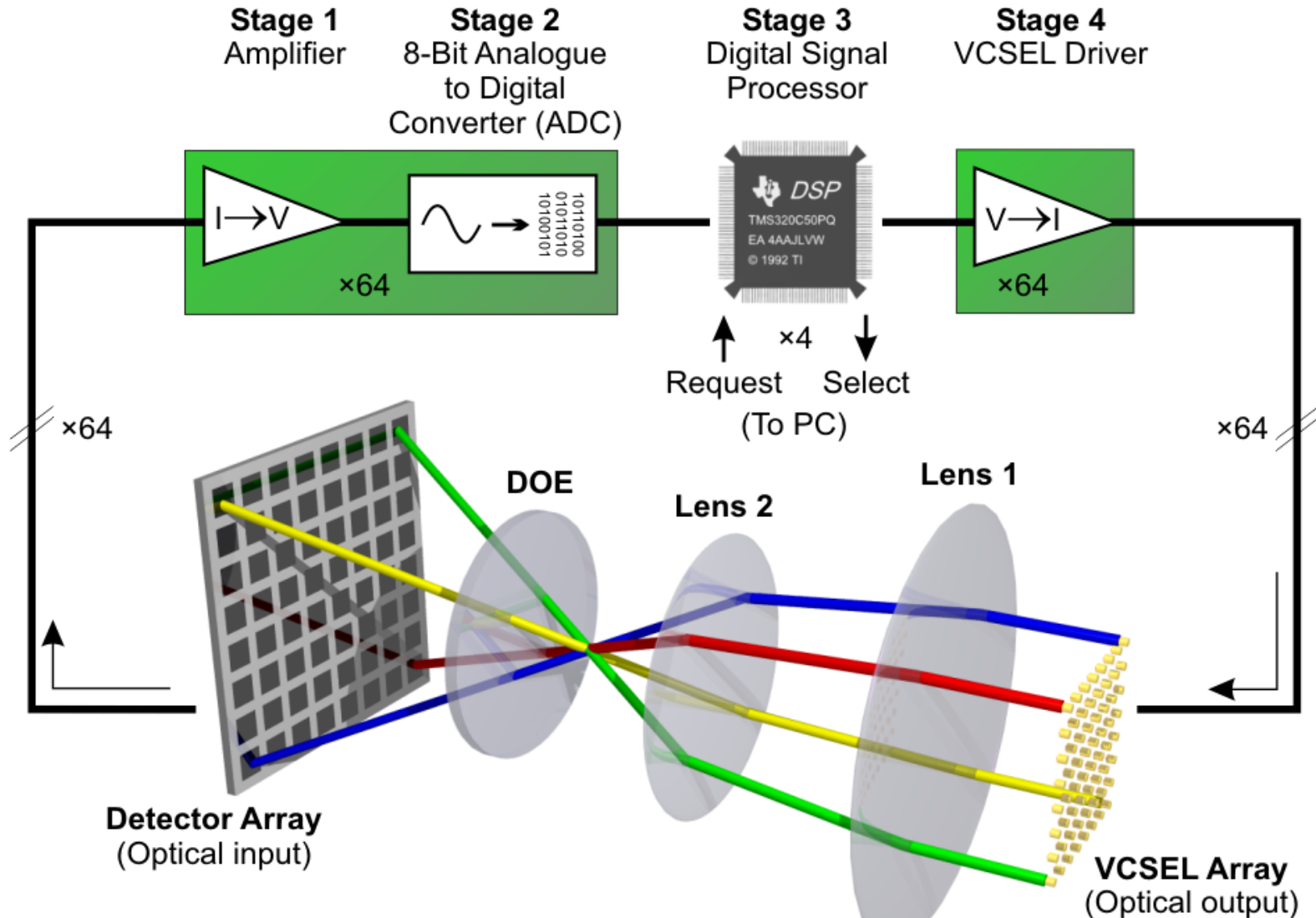
Optical Interconnect



DOE interconnect is space invariant.

Current System

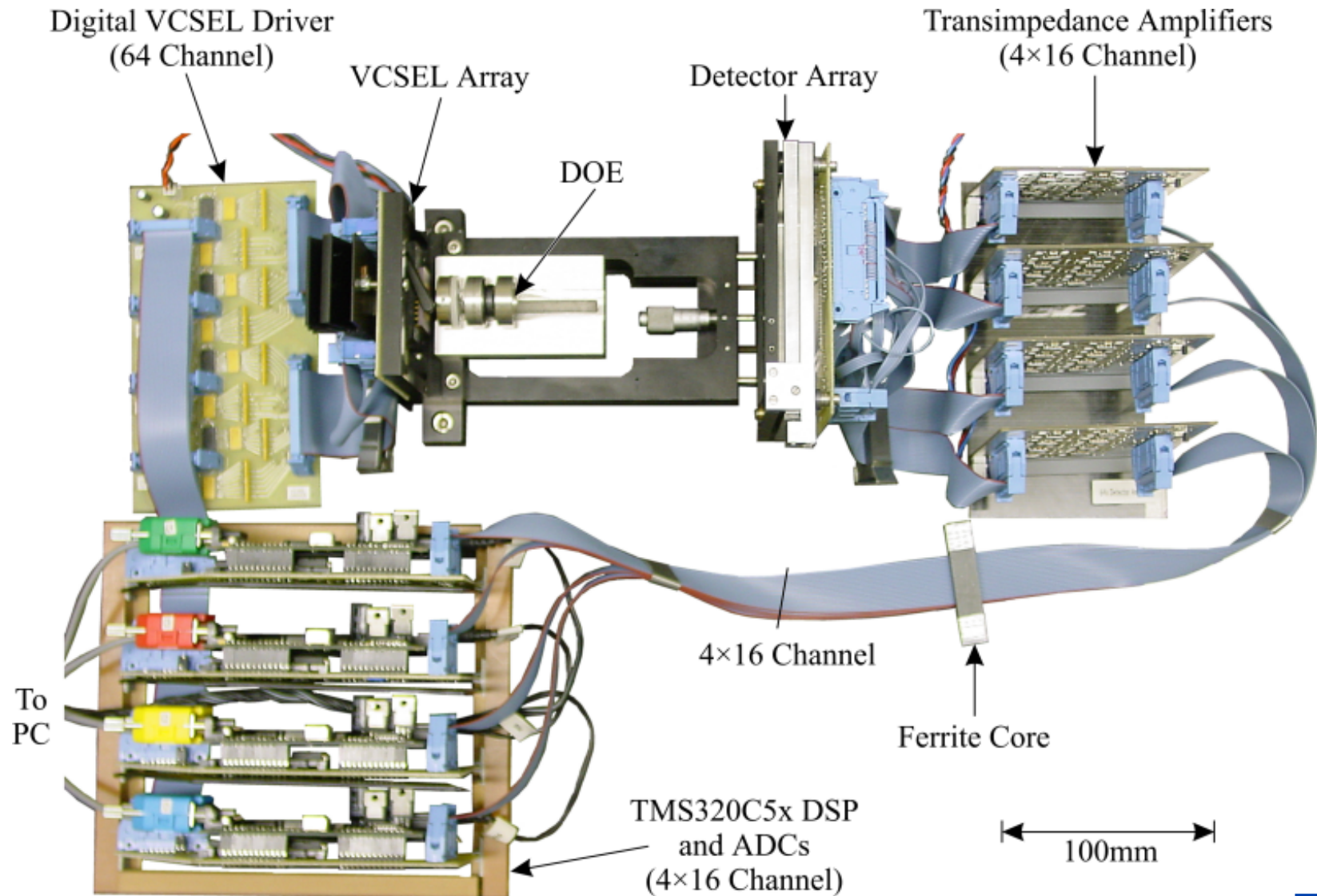
Electronic System



Characteristics

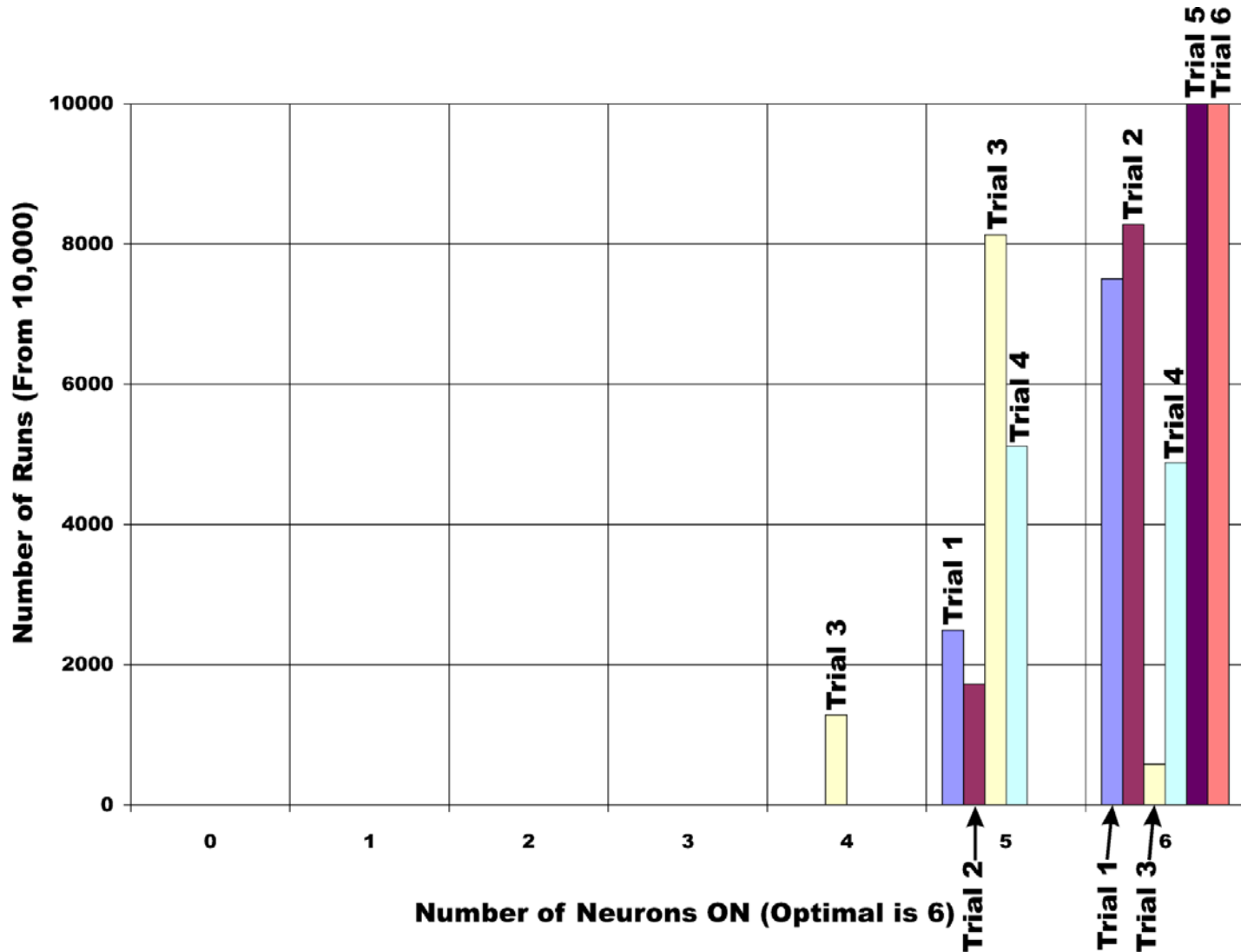
- System uses 4×40MHz Texas Instruments 320C5x DSPs.
- DSPs perform transfer function.
- Transfer function fully programmable.
- Balance of analogue and digital hybridisation can be adjusted.

Actual System

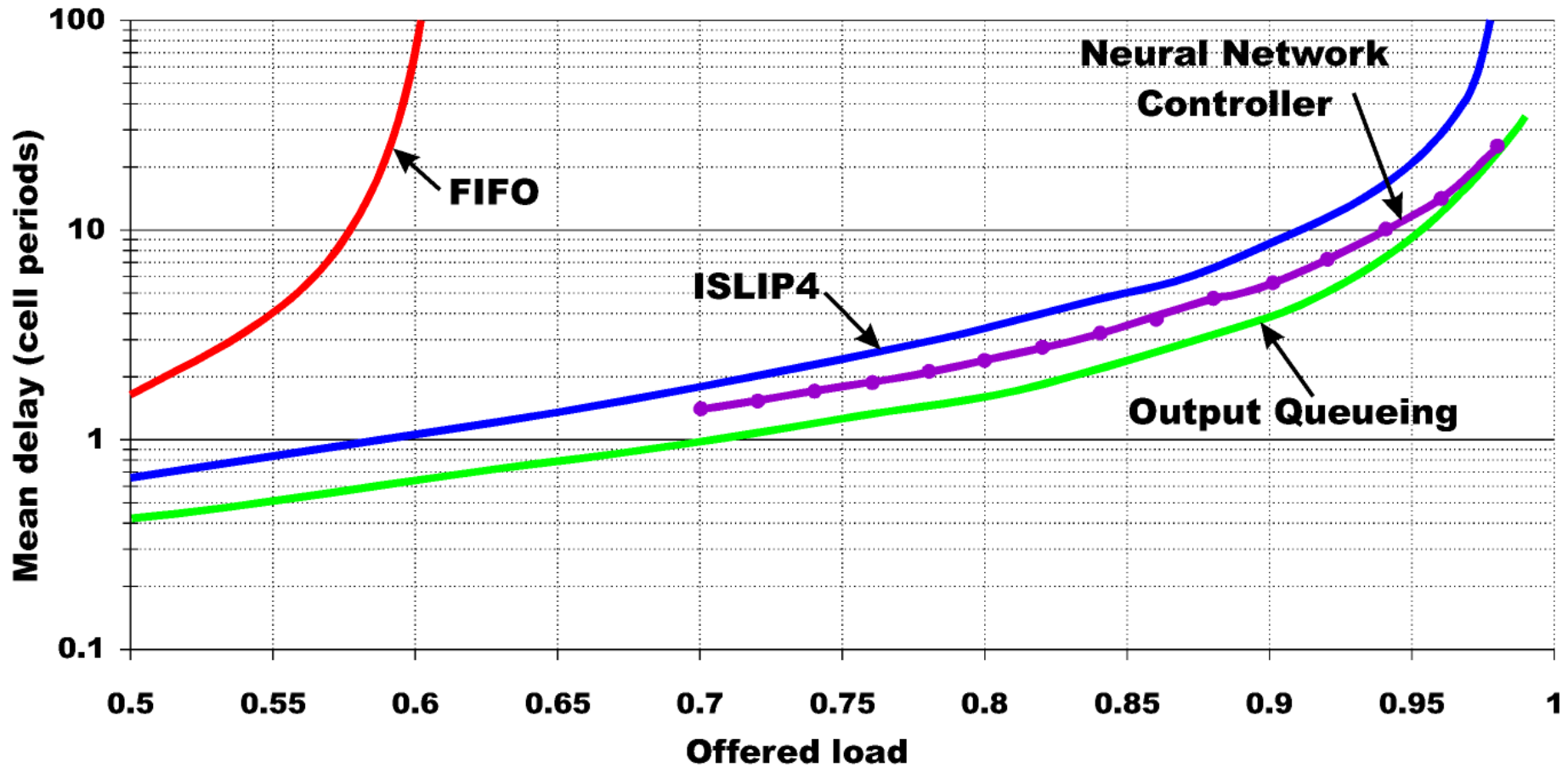


Crossbar Switch Results

Histogram of packets routed successfully in a crossbar switch.

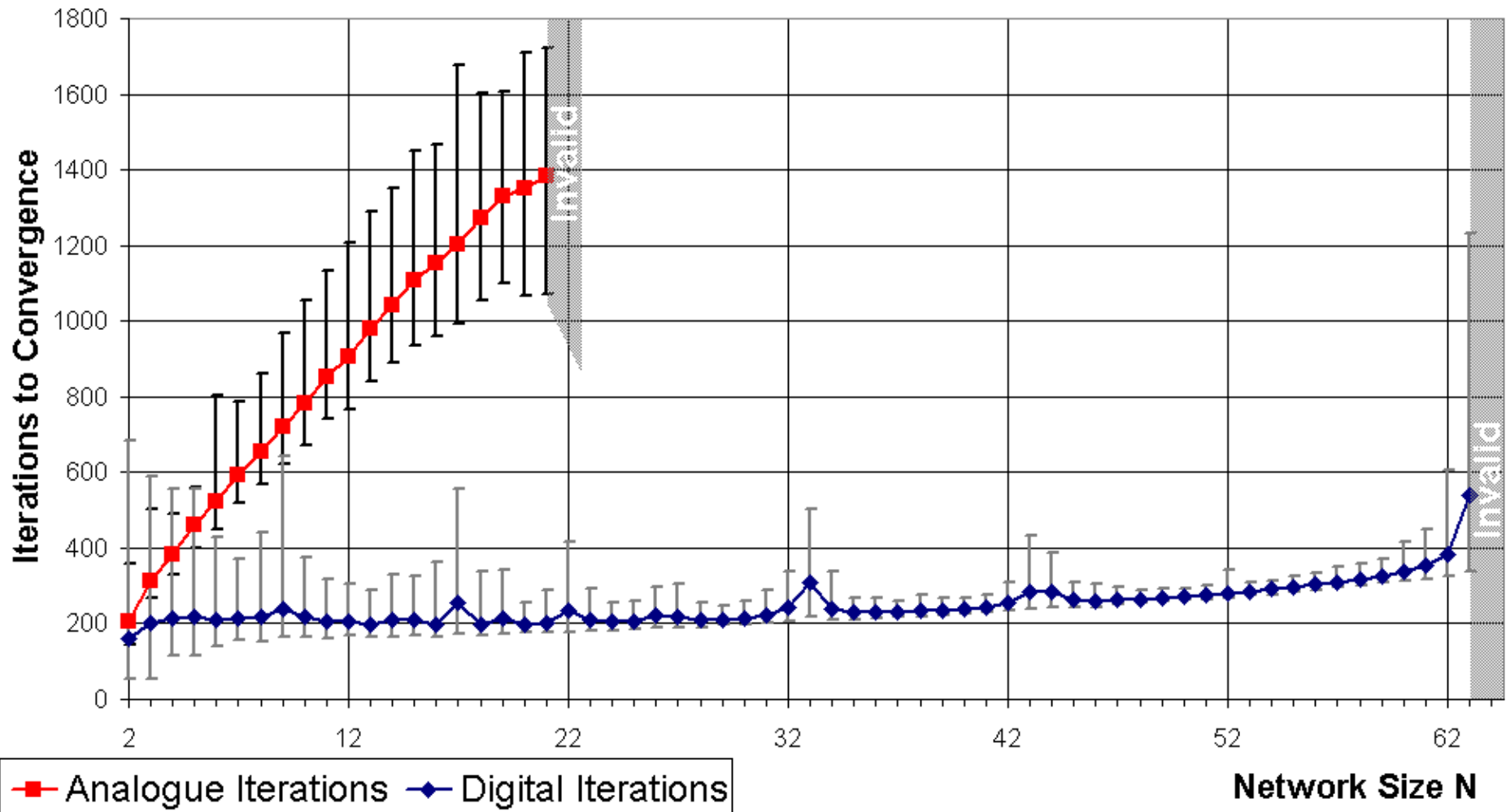


Mean Packet Delay



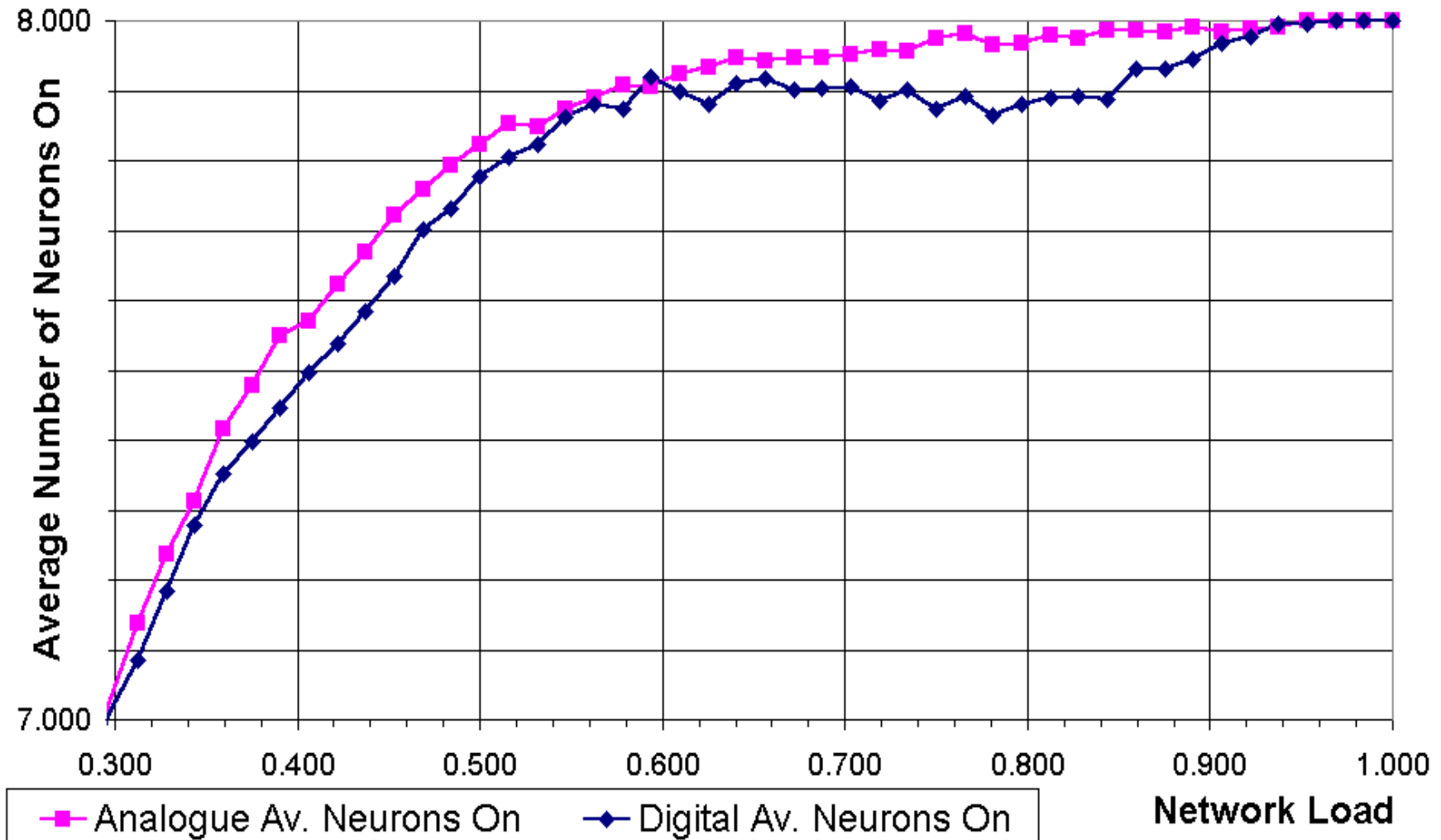
System Scalability

Iterations to Convergence Against Network Size N



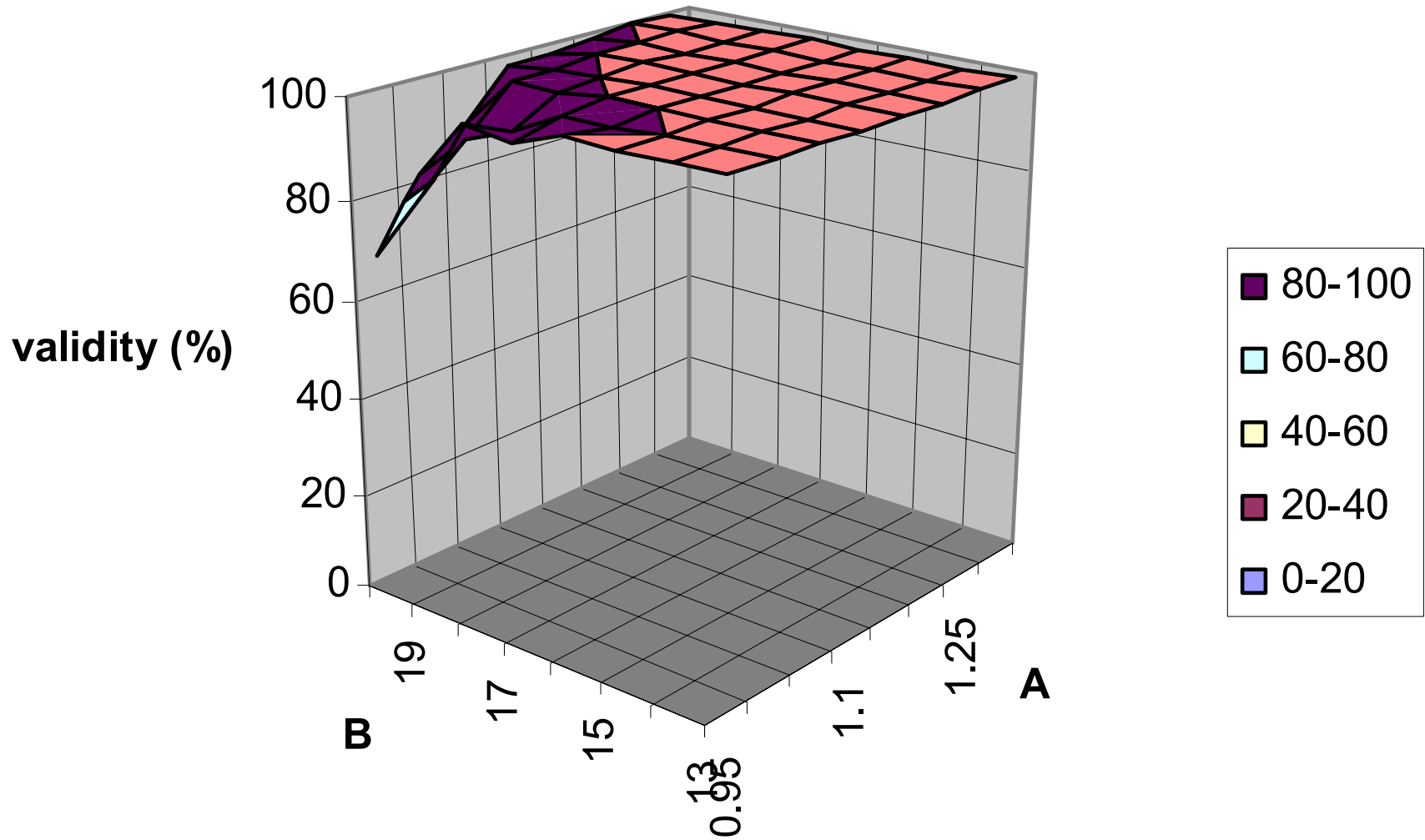
Digital vs. Analogue

Comparison of Digital and Analogue Drivers

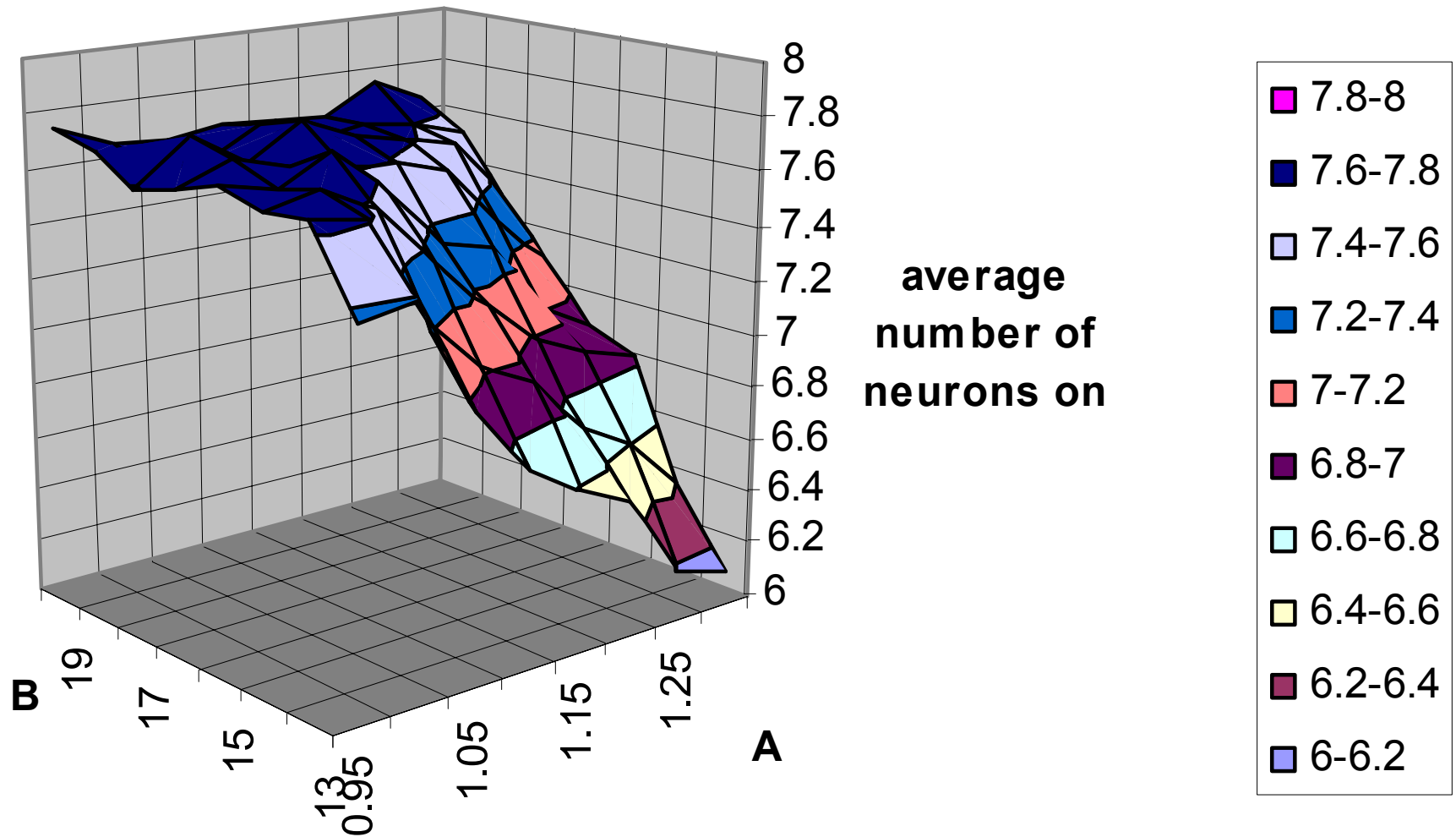


Analogue: Optimal ~97%. Digital: Optimal ~91%.

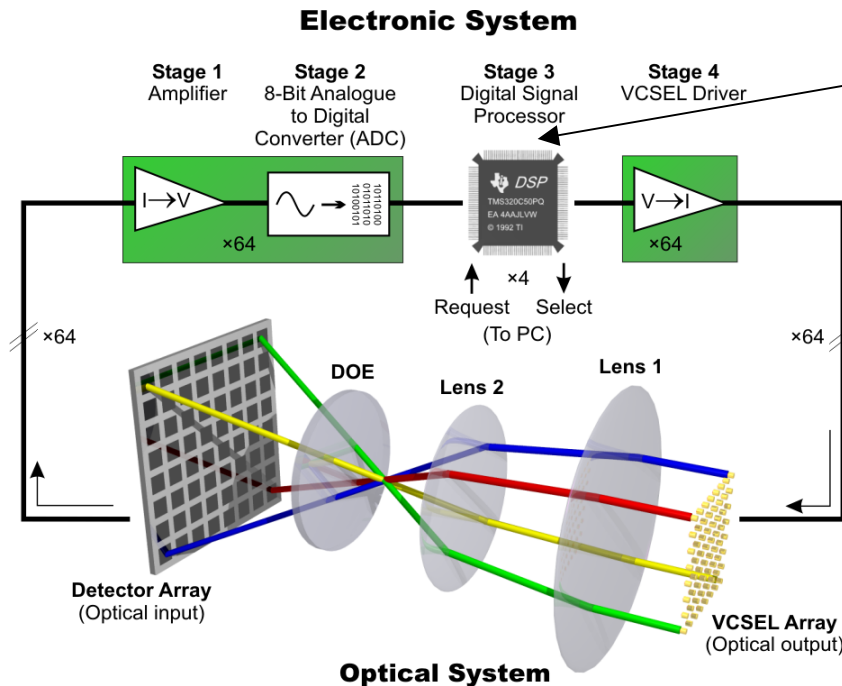
Crossbar Switch Validity



Crossbar Switch Optimality



Control loop optimisation



Control system currently operated in software with test sets

Parameters A,B and C/2 can be adjusted to find point of maximum optimality within the valid region.

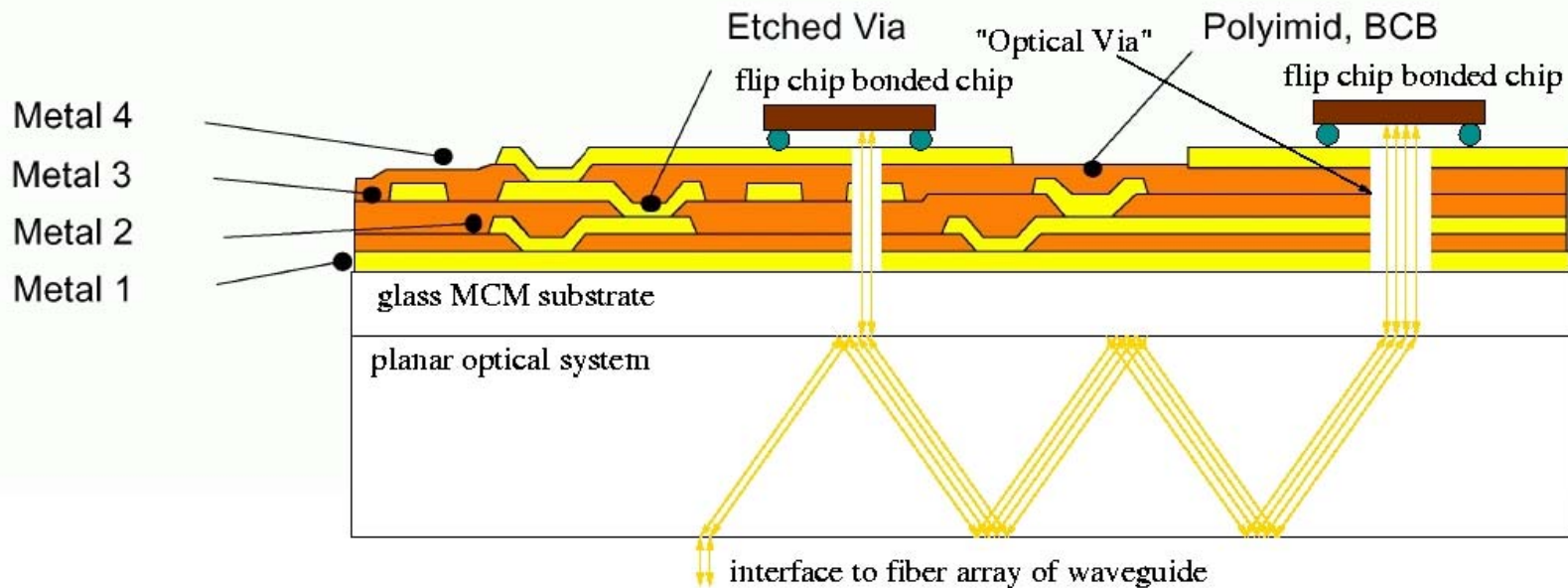
Control system also used for calibration, fault tolerance and diagnostics (e.g. alignment, finger prints on DOE etc.)

General Purpose Operation

- Algorithms can be changed by changing DOE elements.
- King, Queen and Knight problems performed
- Noise removal and labelling
- Correlation, FFT
- General purpose digital or analogue machine (but not necessarily efficient unless mapping is good).
- Some algorithms require complex synchronisation of steps and “superiterations”
- Use of adaptive optics/weights possible.

Multi-Chip Module (MCM)

- The MCM contains:
- Optoelectronic interface chips (LD and PD)
- Electronic driver chips (for LD)
- Transimpedance amplifiers (for PD)



BCB Process: Spin + Photolith. gives higher interconnection than standard PCB implying smaller packages.

Conclusions 1

- System works completely and delivers good solutions
- Performance of 1GHz and higher feasible.
- A digital system running at 1GHz could supply 2.5 million switch configurations per second.
- Scalability mainly limited by VCSEL array size ($N=8$) - system copes well with noise and poor SNR.
- Scalability independent of number of inputs/outputs (N).

Conclusions 2

- Very simple -fixed identical weights.
- Simplicity implies very high performance can be reached.
- Can be general purpose machine - several algorithms run.
- It really does work.
- Further work: *Packaging and integration (maybe HOLMS MCM solution)*, customised electronics/FPGA? Adaptive optics/weights.