Optoelectronic Neural Networks for Packet Switching

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At the core of some of the latest generation of internet routers is a hardware switch that transports packets between the line cards. A central scheduler is required to select a set of packets from queues on the line cards that can be connected to the correct outputs simultaneously without blocking [1]. The larger the set chosen, the greater the throughput, but the decision must be made within the cycle time of the switch. This assignment of outputs to inputs subject to constraints imposed by the switch fabric is an example of a resource allocation problem which can be solved by a neural network [2].

The neural network uses a two-dimensional array of neurons to represent all possible input to output connections. In the case of a crossbar switch, the neurons correspond directly to the crosspoints of the switch. In this type of switch the pattern of neurons inhibited by a given active neuron is shift invariant. That is, it remains the same relative to the position of the active neuron. Shift invariance makes optical implementation especially efficient because the same optical system provides independent paths from all lasers to the appropriate detectors. An electrical system would require a separate wiring network for each output resulting in a highly complex metallisation process. Self-routing (SR) switches can also be scheduled by the neural network with slight interconnect modification to prevent internal blocking at intermediate switch stages. These modified interconnects can also be made shift invariant if the switch outputs are rearranged: in this case in bit-reversed order.

We have implemented a neural network as a parallel optical system using a diffractive optic element (DOE) [3] where each of the neurons has an input detector, followed by neuron circuitry and an output which drives a vertical-cavity surface-emitting laser (VCSEL). Its performance has been measured as a scheduler for both crossbar and self-routing switch fabrics. The experimental scheduler never produced an invalid result. Most of the time it found an optimal result except for certain sequences where it usually routed one fewer packets. Simulation of the neural network, and comparison of performance with other schedulers such as ISLIP4 [1], indicates that it is highly favourable with throughput loads from 70% upwards.

No attempt has been made to make this demonstration system run fast which currently has a decision time of 33μs. Using standard components, it should be possible to obtain results in tens of nanoseconds and achieve scheduling decisions at a rate compatible with the latest router requirements. Designs have now been produced for a smart pixel based system and an enhanced demonstrator, currently under construction, which has increased functionality in that it is able to prioritise input queues.

1. "Tiny Tera: a packet switch core," N. McKeown et al.,
2. "A neural network approach to studying the switching problem," S. J. Amin, S. Olafsson and M. A. Gell, *BT Technology Journal,* **12**, No. 2, pp. 114-120, April 1994.
3. "Synthesis of High Efficiency Diffractive Optical Elements", J.M.Miller, Ph.D. Thesis, Heriot-Watt University, 1993.