Optoelectronic Architecture

for a Dual-functional Neural Switching Optimiser

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Abstract

This thesis presents the optical, optoelectronic, and optomechanical design and describes a novel optoelectronic implementation of dual-functional neural networks for switching optimisation. The demonstrator consists of electronic and optical subsystems. The electronic subsystem employs digital signal processors and analogue/digital converters for Hopfield neural networks to optimise decisions on the throughput of crossbar and self-routing switches. The optical subsystem which holds an 8×8 array of vertical-cavity surface-emitting lasers, photodiode detectors, and a diffractive optical element has been mounted on an optomechanically-designed baseplate whose packaging scheme facilitates focus adjustments and mechanical and thermal stability. The free-space optical architecture exhibits a scalability of the neural networks. It can achieve two different functions with minimal realignments of diffractive fan-out elements. The optomechanical package accommodates all the optical components within a miniature space of approximately 12cm×15cm×25cm. Interconnection theory and optoelectronic components are also covered.

Chapter 1

Introduction

1.1 Overview of the thesis

This thesis begins with a brief description of optical networking and analogue and digital optical computing and describes a list of optical and electronic components. Then it proposes a novel architecture of a switching optimiser by the use of free-space optical interconnects and Hopfield neural computation technique. Finally it concludes with an implementation of the prototype of an optoelectronic neural switching optimiser that could be potentially deployed in the transport for high-speed concatenated data paths and an evolution to optical networking transport infrastructure or what they call Optical Internet.

This thesis is organized as follows: Chapter 1 describes some introductory background on optical networking in Section 1.2 and reports recent developments in

analogue optical information processing in Section 1.3 and digital optical computing in Section 1.4. Neural computation and interconnection theory are covered in Chapter 2. Chapter 3 discusses some critical components for free-space optical interconnection system such as diffractive optical elements, free-space optical interconnects, vertical-cavity surface-emitting lasers, and photodetectors. Chapter 3 also raises a case study of the Smart-Pixel Opto Electronic Connections (SPOEC) project. Chapter 4 presents the design and progress in implementation of the demonstrator. Finally Chapter 5 summarizes the proposal design and concludes this thesis.

1.2 Optical networking

The exponential growth of the Internet has led to similar growth in the capacity requirements for Internet backbones. This makes Internet service providers move quickly to find the most expedient technology for link interconnection between their backbone routes. Increasingly, the technology of choice has been becoming optical networking. Optical networks can take manipulating streams of information by a colour, or a wavelength, thanks to the rapidly advancing dense wavelength division multiplexing (DWDM) technology.

The technology can carry information in the optical domain before dropping it into the electronic domain very far without the conversion of signals between the optical and electronic domains. One of the primary advantageous concepts of optical networking technique is trial to remove this conversion process in which the traffic needs to be multiplexed, routed, and regenerated and takes a toll in terms of complexity and cost as well as speed.

The applications driving a seemingly infinite appetite for optical fiber bandwidth as seen in the doubling of Internet traffic every three or four months all take off from a platform of silicon and software. Perhaps the most amazing is the fact that the expansion of optical fiber transmission capacity has moved even faster than improvements in the processing power, memory capacity, speed, and functions of silicon devices. Today, many interesting materials have been developed and glass fiber is the chosen transmission medium for high-speed, high-reliability, and long-distance terrestrial and submarine communications. Currently bit rates of up to 40 Gbit per second are used in a single fiber. With DWDM, the aggregate bandwidth has exceeded the terabit per second. DWDM systems with up to 128 wavelengths have been announced and DWDM with 206 wavelengths has already been experimentally demonstrated. A40-wavelength DWDM system, at 10 Gb/s per wavelength has aggregate bandwidth of 400 Gb/s – a bandwidth than can transport in a single fiber the contents of more than 11,000 volumes of an encyclopaedia in a second. DWDM systems with 40 Gb/s per wavelength have been already been announced and the trend continues to increase both wavelength density and the bit rate [1] [11].

1.3 Trends in analogue optical computing

1.3.1 Analogue optical information processing

The entire subject of optical information processing or optical computing is too broad to be fully treated here. This section limits the purpose to a presentation of some of the most widely used applications in analogue optical information processing [26]. Some examples of those applications are found in the discussion of pattern

recognition in Subsection 1.3.2 and correlators in Subsection 1.3.3 and analogue optical neural networks in Section 1.3.4. The subject of digital or numerical optical computing was excluded and mentioned in Section 1.4.

1.3.2 Pattern recognition

A particular application of analogue optical information processing that has been of interest for many years is found in the field of pattern recognition. This application affords an excellent example of desired processing operations with simple impulse response but not necessarily simple transform functions. Historically the concept of pattern recognition derived from the field of the matched filter and its application to signal detection [71]. In the present, the concept has spread over many unconventional applications including character, face, and object recognitions. Some of latest achievements in this field follow.

For the application to genome pattern recognition, an analogue optical information processing method for data matching was presented by Tanida et al [22]. With encoding one-dimensional data into spatial code patterns, moiré fringes between two different coded patterns provide information on the correspondence of the original data, which is useful for string alignment in genome analysis. A new code set for the spatial coding is capable of processing complementary base-pairing DNA sequences. The method was implemented by optoelectronic systems that consist of vertical-cavity surface-emitting lasers, a spatial light modulator, and photodetectors and demonstrated the capability of genome pattern recognition.

Horache et al [5] reported the feasibility of coding by coherence modulation in two-dimensional optical signal correlator using a spatially and temporally incoherent light source for real-time multichannnel pattern recognition under natural illumination.

This achromatic system allows to computes simultaneously two cross-correlation products.

1.3.3 Optical correlators

The widely used correlation method for performing complex filtering using a spatial carrier for encoding amplitude and phase information is due to Weaver and Goodman [71], and has been known as the joint transform correlator (JTC). Optical correlation filters used in real time problems are often implemented with ferroelectric liquid crystal spatial light modulators (SLMs).

Inaba at el [8] developed a compact parallel optical joint transform correlator using four binary zone plate array (BZPA) as a Fourier transform lens. This correlator was implemented for face recognition with database of 100 persons using a method of lessening the dependence of JTC on the image size, normalizing the face size by fixing and calculating the three points at two eyes and nose. Although it successfully discriminated the registered facial images from the unregistered facial images, one expected problem in any commercial point of view is the length of time to operate the desired face recognition. Because the length of time largely depends on slow response times (approximately 30ms) of liquid crystal SLM and CCD and the overall operation could take long time.

1.3.4 Analogue optical neural networks

Optical neural networks have attractive feature like massive parallel processing and learning capability for applications in recognition, speech, vision, and robotics. A large number of analogue optical neural networks have been proposed and the selection of different optical devices for weighted interconnections between neuron is

of critical importance. This section describes neural networks using those different devices such as photorefractive crystals, holograms, and liquid crystal spatial light modulators.

An optical neural network using a Pockels readout optical modulator (PROM) has been implemented to recognise three faces after iteration of learning with back-propagation algorithm by Mori at el [10]. Its interconnection weights are written on the PROM, a high-resolution optically addressable spatial light modulator with memory, addition, and subtraction abilities. Similarly the method of using artificial neural networks has been applied to character recognition [9]. However, those applications need to be significantly improved for commercial applications in that the number of characters and faces that they attempted to recognize is 3 or 4 and is too small compared to electronic neural networks.

Frauel et al have shown that interconnection weights are also implemented with holographic interconnects inside a photorefractive crystal for neural networks to perform a Kohonen topological map [3].

1.4 Trends in digital optical computing

1.4.1 Definition of digital optical computing

The integration of larger numbers of primitive computing elements (switches, transistors, gates, processors, etc.) to constitute computers with greater processing power requires the use of interconnects. The silicon fabrication technology has been favoured by the industry because it makes integration look so easy with a millions of

electronic elements on a chip and leap after predictable leap in functionality, performance, and power. On the other hand, the integration of optoelectronic or photonic elements in compound semiconductors used to be quite difficult. However, since a large number of publications brought a widespread attention to the potential in the field of interconnections by the use of optics for the sake of overcoming the communications bottleneck and crosstalk within electronic computing and communication systems, the analysis, design, and demonstration of devices, materials, and components for optical interconnections has become a sub-area of optics called optical computing.

Due to many unique advantages, such as large-bandwidth capability, freedom from electromagnetic interference, and three-dimensional free-space propagation ability, the field of optical computing has great potential for handling parallel communications over electronics. It is then logical to pursue approaches that utilize electronic switching together with optical communication capabilities to construct next-generation high-bandwidth infrastructures. Owing to the intrinsic overlap with respect to the devices, architectures, and even systems employed such as permutation network, some of this research has also taken place under the sub-area known as photonics in switching [2][4][16][15][17].

Some examples of applications in the subject of digital optical computing are found in the latest achievements in waveguide interconnects in Subsection 1.4.2 and optical storage in Subsection 1.4.3. Free-space optical interconnects are among the most extensively investigated subjects in digital optical computing and are excluded from this section and mentioned in Section 3.3 as they are directly relevant with the demonstrator.

1.4.2 Waveguide interconnects

Waveguide-based interconnects have to minimize coupling losses as well as attenuation during transmission. These systems may be based on silica fibers, polymer or Si waveguides if operating at wavelengths above 1 μm. For shorter wavelength optoelectronic interconnects, fibers and polymer waveguides can be used, but the absorption of the Si results in a strong attenuation. Due to the limited space available especially in two-dimensional arrays, single mode waveguides should be used rather than multi-mode waveguides. Furthermore image fiber bundles can be used to reduce the size of the optical pathway systems. In order to simplify the emitter-fiber alignment and the emitter-detector alignment, micro-mechanical fabrication technologies will be used. Waveguide approaches may be better suited to cope with the limited space. In addition polymers may allow using very simple micro-fabrication technologies like the direct exposure of waveguides. However, attenuation and ageing effects that may be significant in polymer waveguides have to be investigated.

A large number of optical waveguides to provide interconnection and filtering has been investigated and they are now ready to leave the laboratory and enter into commercial applications [7]. Various waveguides based on different materials have been studied. They include glass on silicon, plastic, III-V semiconductors. Some of significant and latest developments are mentioned here.

Researchers at LETI in Grenoble developed two waveguides [24] [25]. The first is a Si_3N_4 core surrounded by SiO_2 with lateral confinement achieved by etching a rib on the top surface. They have used this layered structure to fabricate high quality Fresnel lenses and other components and to demonstrate an integrated displacement sensor

and an optical spectrum analyser. Their second waveguide is a channel guide of doped SiO_2 surrounded by SiO_2. All layers are deposited by plasma enhanced chemical vapour deposition (CVD). This technique has been used to fabricate an integrated 4 channel multiplexer with an etched Fresnel mirror.

Workers at NTT developed "high silica technology" in which thick layers of SiO_2 are deposited on silicon by flame hydrolysis, a method originally developed for fiber perform fabrication [13] [21]. This method is capable of depositing layers of order 100 μm thick. Multimode waveguides with 40 × 40 μm cores and single mode waveguide with 8 × 8 μm cores are formed. Their single mode design has been applied to the fabrication of an integrated four channel Mach-Zehnder multiplexer with approximately 1A channel spacing and thermal tuning of the channel wavelengths [14][23].

Recently researchers [20] at Heriot-Watt University have developed a low-loss multimode planer waveguide circuits using direct write of polymers. Rapid direct writing of the waveguides and other structures is realised using a high-power 325 nm He:Cd laser. Mesurements of loss with different laser sources has shown that the guide loss is less than 0.5 dB/cm at 1300 nm and less than 0.17 dB/cm at 850 nm.

Laser direct writing techniques for the fabrication of single mode waveguides have been published since 1996. The single mode waveguides had performed an attenuation of 0.02dB/cm at 840 nm. However only very short waveguides (2–5 cm) had been realised. Moisel at el have used an improved direct writing technique that allows fabricating multimode polymer waveguides. They have cross sections of approximately 250 μm x 250 μm and can be fabricated up to 55 cm length with an attenuation of 0.03dB/cm [18].

Griese [6] raised manufacturing requirements of optical waveguides integrated upon printed circuit board. To be compatible with the existing multi-layer board manufacturing process, those interconnects should be a part of a passive optical layer.

1.4.3 Optical storage

Optical and volume holographic storages have the potential to provide large capacities based on the novel ability to multiplex many holographic pages within a given volume. A variety of recording methods and materials have been demonstrated. In holographic storages, pages of information are overlapped in the volume of the recording materials. Due to destructive read-out of holograms in photorefractive materials such as $LiNbO_3$:Fe, holograms had to be recorded with an exposure schedule in order to equalise diffraction efficiency proportional to $1/M^2$, where M is the number of exposures. Researchers at Caltech [19] used a non-destructive read-out in doubly-doped $LiNbO_3$ to improve the diffraction efficiency with the $1/M^2$ dependence and recorded 50 localised holograms.

Other type of recording technique is a two-photon absorption process. In this process laser beams are focused inside the media, the photochromatic compounds will be excited by the sum of two photons energy at focus where the laser intensity is high above the two-photon absorption threshold. Once excited, the material transforms into another form which will emit fluorescence when excited again.

In the experiments by Zhang et al [27], a frequency-doubled Nd:YAG laser and a high repletion rate (76MHz) short pulse (250fs) mode-locked Ti:Sapphire laser have been used to store data in multi-layer volumetric media. It was concluded that one 5.25 inch two-photon three-dimensional optical disk with 10mm thickness could have over

500GB capacity with the aberration compensation and dynamic recording with damage control.

Chapter 2

Neural Computation and Interconnection Theory

2.1 Introduction

This chapter covers the computation technique using Hopfield neural networks in Section 2.2 and their application to two types of switching fabrics (crossbar switch in Subsection and self-routing switch) in Section 2.3, and argues on what type of optical interconnections should be employed most preferably, based on interconnection theory by use of a flow chart in Section 2.4.

2.2 Hopfield neural networks

2.2.1 Neurons and interconnections

A Hopfield neural network consists of a large number of threshold processing elements called neurons shown in Figure 2.1, and inhibitory interconnections between these neurons [29] [34] [35] [49] [50]. By careful selection of the inhibitory interconnection pattern the network can be made to optimise some arbitrary function.

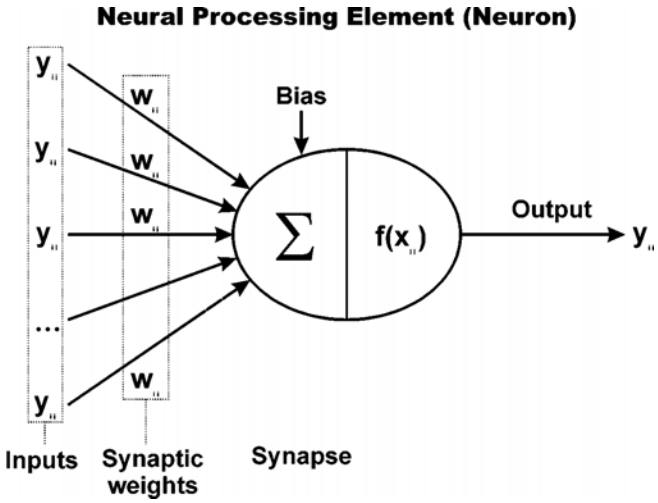


Figure 2.1 Schematic diagram of an artificial neuron

Neurons are the basic building blocks of neural networks and are an approximation of the neuron found in nature. A neuron takes inputs from the outputs y_{ij} of other neurons and multiplies their strengths by a scalar weight w_{ij} known as the synaptic weight. The neuron sums all inputs along with a specific bias to find x_{ij}. The output y_{ij} of the neuron can then be determined using a monotonic activation function

$$y_{ij} = f(x_{ij}) = \frac{1}{1+\exp(-bx)} \qquad \text{(Eq. 2.1)}$$

Here the value of b is used to control the gain of the sigmoid function where a higher value results in a steeper transition. The exact form of the activation function is not particular important and in practice any appropriate monotonically increasing nonlinear function could be used.

Adapting a neural network to any problem requires that an updating rule is defined and thereby the network interconnection structure. The updating rule determines the next value that a neuron will take with respect to time based upon the previous outputs of other neurons according to the equation shown in Figure 2.2. [50]

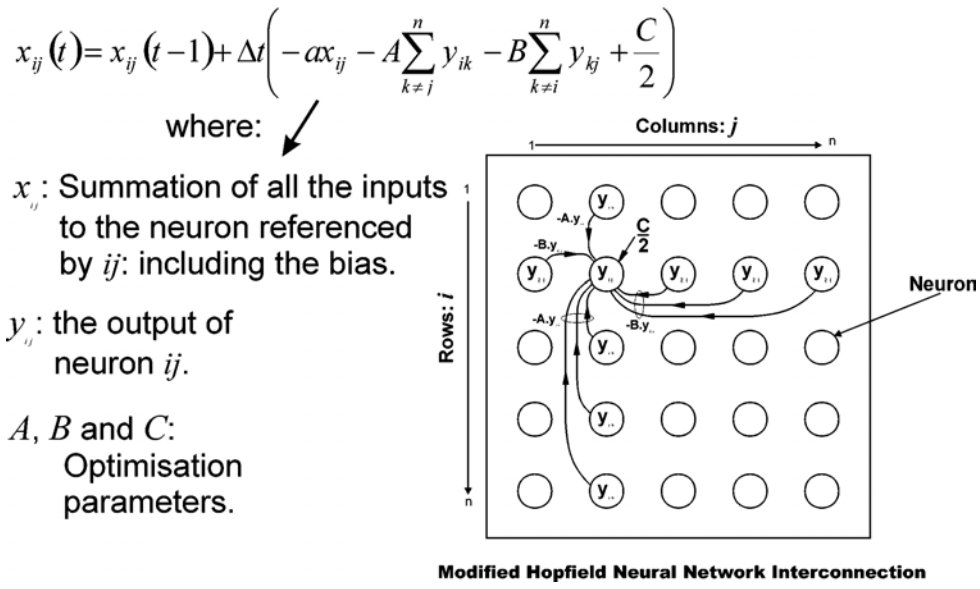


Figure 2.2 Modified Hopfield neural networks

To illustrate this rule further, Figure 2.2 shows an interconnection diagram for the modified system. Here the neuron marked with output y has inputs from all the other neurons in the same row $-B\ y_{2j}$ and column $-A\ y_{i2}$. The important point to note here is that the neural network works in an inhibitory fashion so any active input will inhibit y_{ij}. *C/2* describes the external bias supplied to each neuron that is not inhibitory.

It has been shown by Hopfield that with symmetric connections and a monotonically increasing activation function *f(x)*, the dynamical system described by the neural network processes a energy function which continually decreases with time. The existence of such a function guarantees that the system converges towards equilibrium. The optimisation parameters *A, B*, and *C* [33] have been determined purely by trial and error in previous works [28]. If these parameters are not chosen carefully, then function *x(t)* in Figure 2.2 will converge either very slowly or not at all. A further possible problem is that the system might converge to an invalid solution.

2.2.2 Electronic implementation of a neuron

The structure and the sigmoid response of each neuron can be electronically implemented as shown in Figure 4.3. [124]

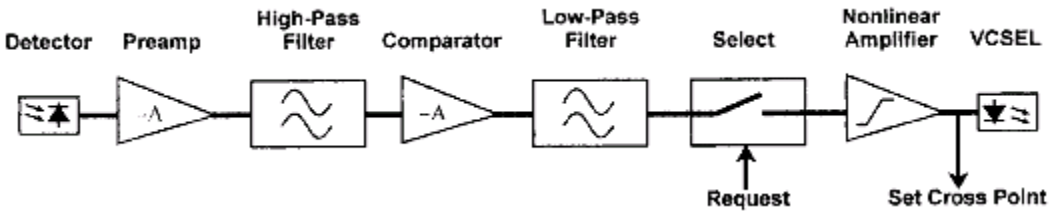


Figure 2.3 Block diagram of an electronic neuron. Each neuron consists of a series of electronic components. This diagram indicates how a neuron is represented in a modular form.

In this electronic hardware implementation, each of the neurons has an input detector that is followed by a capacitor-coupled inverting amplifier chain and a low-pass filter; the output drives a vertical-cavity surface-emitting laser (VCSEL). (For example, the VCSEL array presented in Chapter 4 is 8 × 8, but only 48 neurons could be used. Thus the switch control was a 6 × 8 system.) Figure 2.3 shows the modular electronic layout used to generate the required neuron characteristics. Essentially, this arrangement generates the dynamics and the outputs described by [30]

$$\frac{dx_i}{dt} = I_i\left(-\mathrm{l}_i x_i - \sum_{j=0}^{N-1} w_{ij} y_j + t_i \right) \qquad \text{(Eq. 2.2)}$$

$$y(x_i) = o_{\min} + \frac{o_{\max} - o_{\min}}{1 + \exp(\mathrm{b} x_i)} \qquad \text{(Eq. 2.3)}$$

where x is the state of a particular neuron in time, y is its output, and t is the threshold or the bias for the neuron. The above equations evolve such that x follows a negative exponential with the time constant $1/\mathrm{l}$ to reach a steady state with a well-determined value of y. The value of y is nominally the same for all the neurons. The weights w can be represented by the optical connections through the diffractive optical element (DOE). These weights are also nominally equal and are determined by the attenuation of the optics. In this case it is desirable to maximize the weights. The time constant and t are set by the resistive and capacitive elements, respectively, within the electronics. The filter circuits shown in Figure 2.3 largely determine the time constant in this implementation.

The threshold t determines where the neuron evolution starts on the response curve shown in Figure 2.4. This parameter is also nominally the same for all the neurons and is used to set the initial state of the network in such a way as to optimise convergence. Different values of *t* would be selected for attenuations *w* and different values of b. The variable *I* takes the values 0 or 1 and determines whether a given neuron will be allowed to evolve. This process corresponds to a request for a particular connection. The value of b determines the slope of the activation function as Figure 2.4 and in practice is essentially determined by the gain of the amplifier in the neuron. The terms o_{min} and o_{max} merely refer to the minimum and the maximum outputs, respectively, of the neuron, which in this figure can be seen to be 0 and 1 respectively.

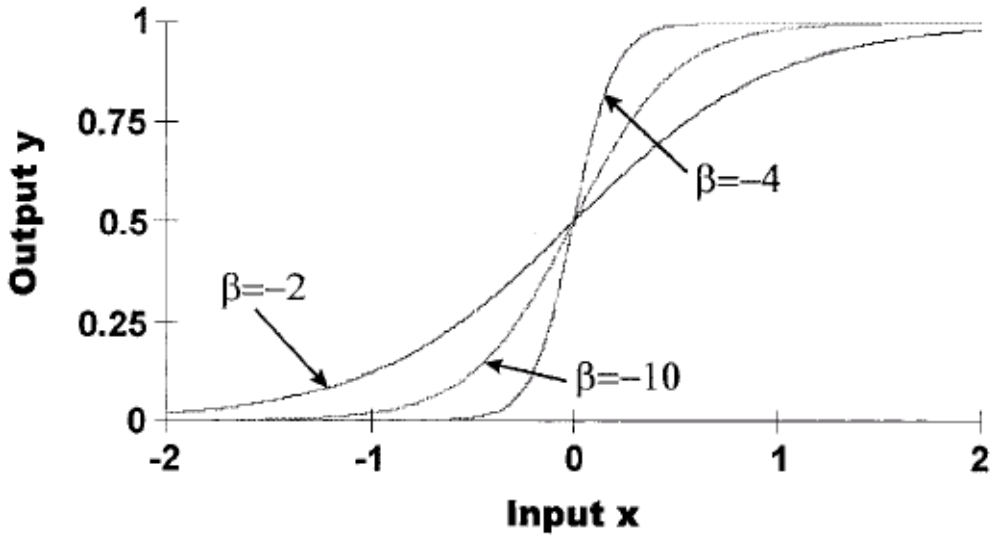


Figure 2.4 Sigmoid response of a neuron: The slope of a neuron's activation function is highly dependent on b. This diagram indicates how the slope changes by use of three values of b.

2.3 Neural computation for switching optimisation

2.3.1 Crossbar switch

This section describes the Hopfield neural network architecture to optimise a crossbar switch in real time in order to effect the switching of packets at very high rates with maximum throughput [30][32][36][38][120][121].

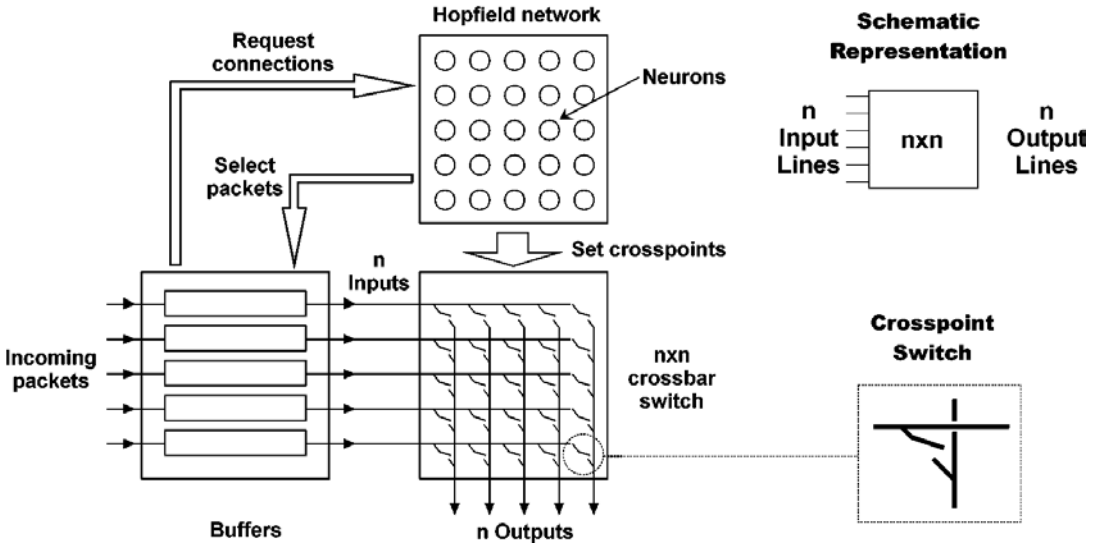


Figure 2.5 Overview of a Hopfield neural network optimiser

The problem of maximizing the throughput of packets through a crossbar switch is illustrated in Figures 2.5 and 2.6, which show how a request for packet transmission through an N × N crossbar can be mapped on to an N × N binary matrix, the input request matrix. For the most common type of packet switching that provides point-to-point interconnection, there should be at most one cross point closed within each row and column of the crossbar when the packet is sent through the switch. The routing of the packets through the crossbar can be mapped onto an N × N binary matrix or the

configuration whose elements indicate which cross points are to be “open” or “closed”.

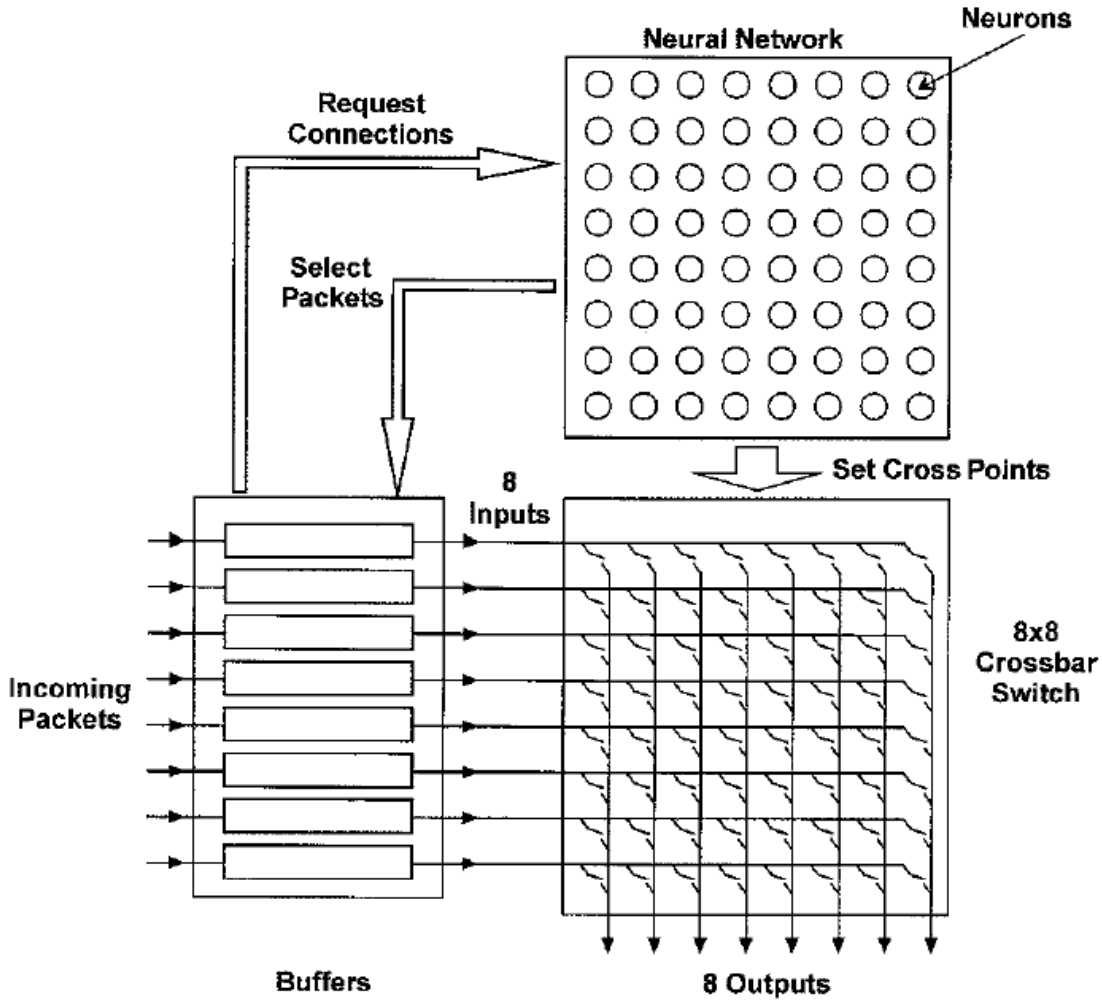


Figure 2.6 Schematic picture of the experimental neural-network optimiser for crossbar switch. On the basis of the connections requested by the incoming packets the neural network chooses an optimal solution, sets the appropriate crossbar switches (cross points), and then selects the packets chosen to pass through.

The problem of maximizing the throughput is to find an optimal configuration matrix or a permutation matrix whose overlap with the input request matrix is maximum.

When each queue manager receives a packet from its input line, it examines the destination address to determine the output line of the destination. It then updates its row request vector by setting the bit of the appropriate column and places the packet in its internal queue. Row request vectors of all queue managers are supplied to a neural network having one neuron for each cross point. The neural network uses the combined row request vectors as its initial state and computers an optimal configuration for the crossbar switch. The resulting row configuration vector is returned to each queue manager, and all cross point in the crossbar switch chosen to be operated are then close. Each queue manager transmits a single packet as selected by the returned row vector through the crossbar switch to the appropriate output and updates its row request vector by clearing the bit of the selected column if no more packets for that output remain. This process continues in a cycle where new packets are being received while queued packets are being transmitted. If all packets are of a fixed length, it is impossible to receive new packets, transmit selected packets and computer the next configuration in parallel.

The combination of an optimal configuration matrix should be executed in less time than it takes to transmit a packet, perhaps as short as a few microseconds for fiber optics communication systems. It should be clear that for large switching systems the calculation of an optimal configuration in such short times by ordinary computing methods is impossible, but neural networks offer a potential to solve such problem due to their rapid convergence if an appropriate set of synaptic weights can be found. In order to tackle this goal, a Hopfield neural network control an 8×8 crossbar based on electronic VLSI circuits has been implemented, but the results concluded that an optoelectronic implementation would probably be more suited for the larger size and

faster switch schedulers in view of the architectural simplicity, i.e., synaptic weights having the same sign and absence of external input currents [38].

2.3.2 Self-routing switch

Next consider the other type of neural network for self-routing multi-stage banyan switch [31] shown in Figure 2.7 [124]. In this case the incoming packets have a header address that determines their paths through the banyan network.

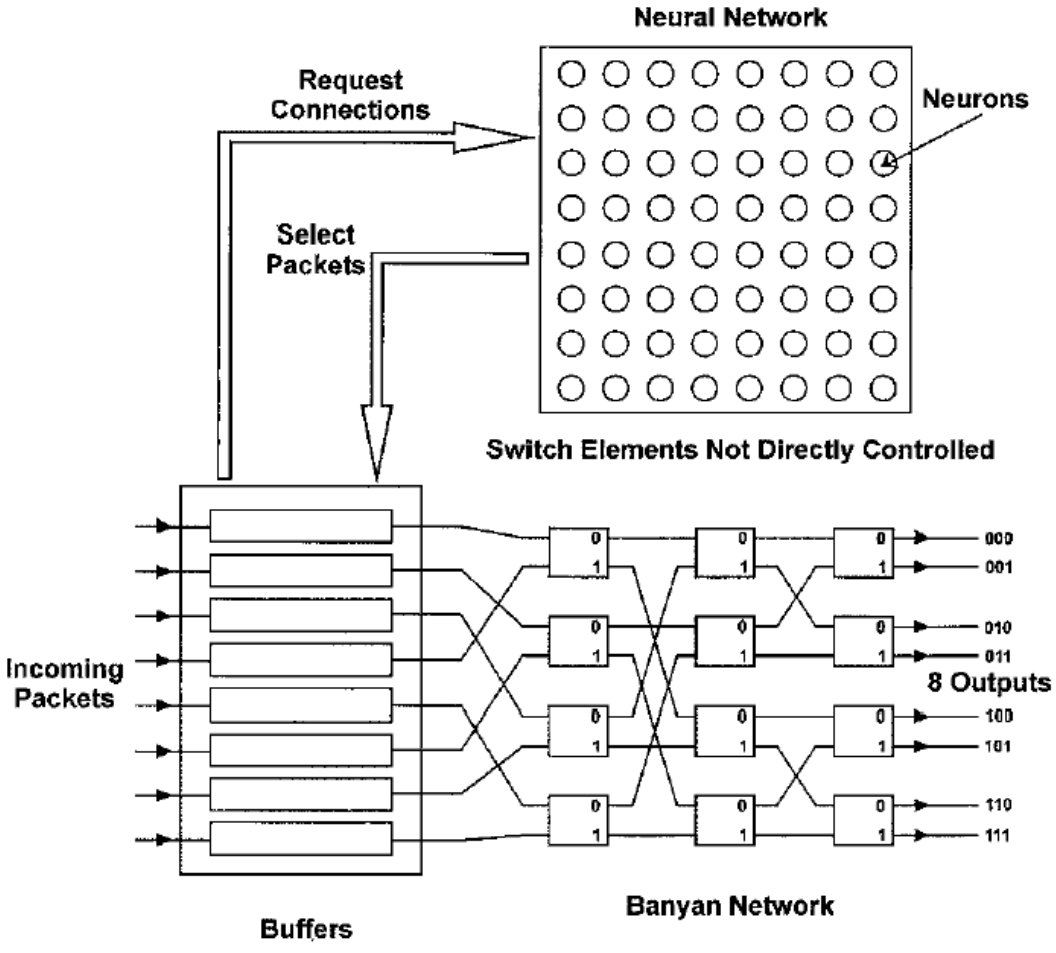


Figure 2.7 Schematic of a neural-network optimiser for a self-routing multi-stage banyan switch. Here the neural network selects an optimal packet solution and notifies the input buffers.

This characteristic has an advantage that the optimiser does not require to set the switches explicitly but merely to select packets to be launched into the fabric. The penalty is that the banyan-type switch shown in Figure 2.7 is internally blocking and the optimiser must perform a more complex task. The neural-network optimiser copes well with this added complexity in that the correct functionality can be attained by the mere provision of additional inhibition paths that provide contention between requests for these blocking configurations. By considering the grid of neurons with the left-hand vertical edge corresponding to the input port of a packet and the lower horizontal edge corresponding to an output port, one can see how this inhibition can be achieved.

2.4 Interconnection Theory

2.4.1 Definition of Interconnection Theory

This section first discusses what is meant by the term interconnection theory in Subsection 2.4.1 and gives some examples of the types of problem it addresses. Then it discusses the various architectural choices for optical interconnections, first considering two-dimensional systems in Subsection 2.4.2 and then moving into three-dimensional free-space architectures in Subsection 2.4.3. Among the various alternatives, this paper singles out a globally interconnected architecture with devices arrayed on a plane in a three-dimensional free-space system as a promising alternative and discusses its benefits.

It is useful to identify a set of mathematical and empirical models, observations, mathematical concepts and tools, and methods of analysis under the title of "interconnection theory" [40]. Interconnection theory is a physical theory of computation based on interconnection-dominated models such as neural networks. It is a physical and architectural theory as opposed to a logical or algorithmic theory in that it deals with the actual physical and material construction of computing systems, with the flow of information through real space as governed by geometrical and physical limitations. Interconnection theory is based on interconnection-dominated models rather than on device-dominated models on the basis of the understanding that computing systems of ever-increasing numbers of components are limited by the problems associated with transferring information within the system rather than with the intrinsic limitations of the devices themselves. It puts them at the central issue of its models. Digital computers consist of the interconnection of nonlinear elements according to a certain graph. Interconnections are physical channels with width, length, energy consumption, delay, and bandwidth. Interconnection theory deals with the resulting system-level parameters such as size, power consumption, and speed and how these are affected by architectural and technological choices.

Choices dealing with the physical aspects of devices, those dealing with transmission lines, interconnections, and packaging, and those dealing with the architectural and logical aspects of computing systems often limit their attention to their own domains. In consequence, the solutions they find are optimal in a narrow sense, in that they may not be the most optimum solutions that would be obtained from a theory that jointly considers all domains at once [61] [62] [63]. However, for certain issues a number of general assumptions may allow us to reach certain results that may be claimed to be

optimal in a wider sense, although they are not obtained from a fully general theory. This assumption is logical when a certain aspect of the problem can be isolated or separated such that consideration of other parts would have no effect on the result anyway.

2.4.2 Two-dimensional system

Three-dimensional systems seems of course better than two-dimensional systems in terms of performance, but since they take up less space there is still a point to comparing two-dimensional optically interconnected systems with conventional two-dimensional electronic systems. Comparisons of the capabilities of two-dimensional optical and electrical interconnections do not significantly favour optics when we allow for active repeating stages in the electrical lines. In electrical systems repeaters can be used without significant penalty.

To determine if it is practically possible to bring the effective interconnection widths down to the order of a few micrometers for complex waveguide circuits, Onal at el [39] have developed computer-aided analysis and design tool to calculate the minimum waveguide spacing in complex circuits of arbitrary rectilinear topology in order to maintain acceptable cross-talk levels. It was found that, as a result of the necessity of avoiding coupling and intrinsic material problems, complex integrated optical waveguide circuits force large effective widths. It was indicated that effective widths could not be easily brought down to a few μm for dense circuits. Therefore one might conclude that optical waveguide circuits cannot compete with electrical integrated circuits when one take in account the fact that scaling of electrical transistors has already been reduced to approximately 0.1μm at present [51].

Nevertheless, as this paper commented above, even in this case the use of two-dimensional optical waveguide circuits offers a noticeable advantage in very limited circumstances. Thus one may conclude that two-dimensional optically interconnected systems will not necessarily find widespread use and immediate enthusiasm among engineers in future high-performance computing systems.

2.4.3 Three-dimensional system

We denote the number of elements, switches, and processors in a computing system by N. We assume that the graphs specifying the connections between these elements are of bounded degree, that is, the number of connections pinouts emanating from each element does not increase with N. We also assume constant or approximately constant power dissipation per element and that the elements are of constant size.
These assumptions are not restrictive but rather are needed to ensure consistency. If we are to compare systems of different sizes and discuss how certain quantities change as system size increases, we must measure the system size in a unit that is constant in processing power, size, number of connections, pinouts, and power dissipation. This unit is what we refer to as an element. For clarity, we concentrate on one-to-one interconnections. We should note that it has been suggested that architectures with one-to-many and many-to-one interconnections may be more advantageous.

Next one can mention about the comparison between the devices arrayed on parallel planes and those arrayed through a volume (or in other words, non-parallel planes).

There is no promising category of volume-shaped or cubic-shaped photodetector and light emitters that should be suited for arraying devices through volume. It has not gathered any enthusiastic investigations in general. Also, it is easily imagined that the process of implementing optical components through volume involves higher level of alignment problems. Therefore one can make a general architectural proposal in favour of arraying on planes against arraying through a volume [40] [42].

2.4.4 Comparison between global and local interconnections

This section compares between global and local architectures. And their different features are summarized in itemized form as follows:

	Globally interconnected	Locally interconnected
Example	Butterfly graph	Mesh graph
Algorithm	A small number of steps	A large number of steps
Physical duration	Long physical duration for each step	Short physical duration for each step

Table 2.1. Different features of globally and locally interconnected architectures

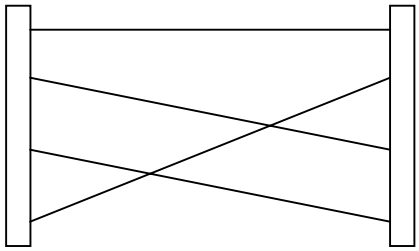
If one employs global architectures, the available connections make it possible to employ an algorithm that computes the answer in a small number of time steps. However, the physical duration of a single time step is long because of the length of the inter-connections. On the other hand, one may employ a locally connected architecture that will require a large number of time steps but in which the duration of the time steps will be short. However, by taking into account that long physical duration for each can be overcome by the use of optics, it is fair to make a general argument in favor of global interconnections in the case of using optics without getting into a discussion of specific algorithms. The use of a globally connected architecture is advantageous in that it allows for one to minimize the number of time steps and realize a higher density of interconnections or, in other words, higher degree of parallelism. But at the same time, it is disadvantageous in that the long interconnections needed may occupy more space, forcing the devices constituting the system far apart and resulting in a large system size and long signal delays.

A globally connected graph is again preferred because of its greater versatility. Certain operations do not demand much connectivity among the elements of the system designed to perform them.

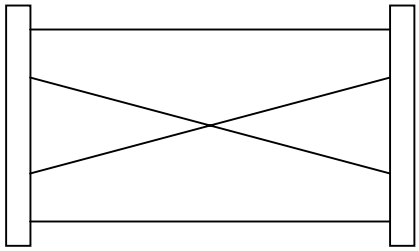
In such less-demanding cases, it might not make much difference whether we use a locally or globally connected system. We are considering the more interesting set of operations or problems that do demand global information flow for their solution.

2.4.5 Comparison between irregular and regular interconnections

In this section the irregular interconnection that provides an arbitrary pattern of connections between two device planes (or arrays) is compared with a restricted pattern of interconnection architecture that can provide only a regular pattern of connections [46].



Irregular



Regular

Figure 2.8 Irregular and regular interconnections

Again, their main different features may be summarized in the following table:

	Device planes with Irregular interconnections	Device planes with Regular interconnections
Pattern of connection	Arbitrary	Restricted
Steps or iterations	Fewer steps	More steps

System size	Large	Small
Connection length (delay)	Large	Small

Table 2.2 Different features of irregular and regular interconnection

The architecture with the regular interconnection pattern may seem restrictive, but a system with such connections can solve the same problems as the other in an indirect manner through the action of shuffling the information back and forth several times. Despite the fact that this system will require a greater number of iterations or time steps to solve a given problem, it will also exhibit a smaller system size. Also the use of the restricted patterns of electronic interconnections have been extensively investigated and already implemented especially in the communication systems, such as crossbar switching and self-routing switching systems. Therefore it is more logical to inherit the past successful implementations of electronic interconnections and apply them to interconnections in the optical domain rather than it is to explore completely new arbitrary patterns of interconnections. In the case of free-space optical interconnection using diffractive optical elements (DOEs), it is more advantageous with regular interconnections. Because irregular interconnections require highly complicated DOE designs and involve more obstacles in mass-production and alignment.

2.4.6 Architectural choices for optical interconnections

After the above-mentioned comparisons in each domain, we can now embark on the main argument. Let us take a look from up to down the flow chart (shown in Fig. 2.9) of alternative choices for optical interconnection in order to chose a single alternative.

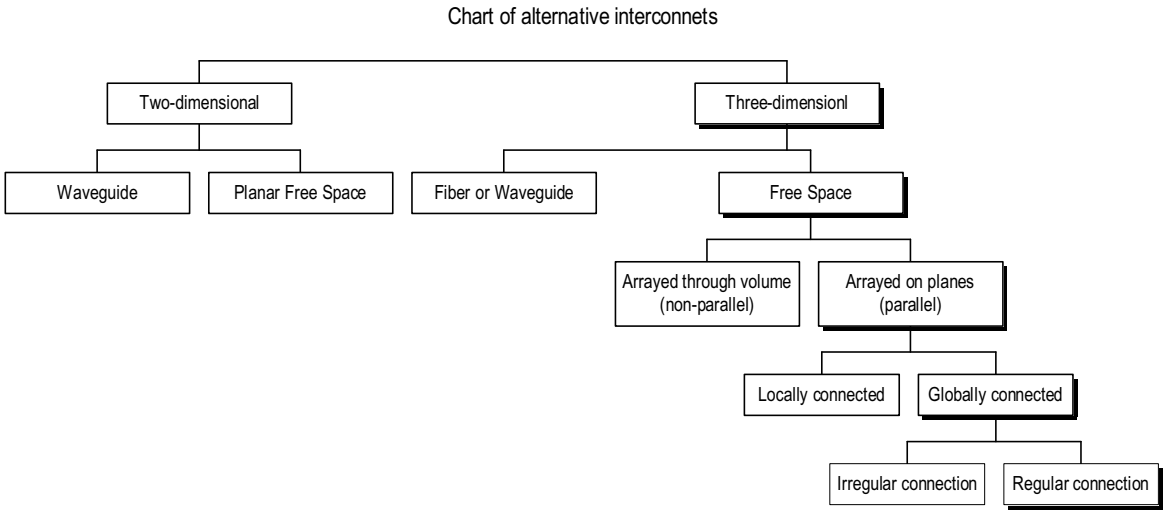


Fig 2.9 Flow chart of alternative interconnection architectures

The labels of the options this section examines are depicted in Fig. 2.9:

Firstly Subsection 2.4.2 section looks at two-dimensional systems and argues that they are of limited utility. After turning our attention to three-dimensional systems in Subsection 2.4.3, it becomes evident that free-space systems offer the best promise. By further examining the alternatives in Subsection 2.4.3, we decide that arraying optoelectronic devices on a plane (or a limited number of planes) is preferable to

arraying them throughout a volume (or non-parallel planes). On comparing locally and globally connected systems in Subsection 2.4.4, we decide that globally connected systems are preferable. We further argue in Subsection 2.4.5 that globally connected systems based on regular connection patterns constitute the best choice. (Note that a system is considered superior to another if it can finish the same task in a shorter amount of time or finish a larger task in the same amount of time and cost may similarly be factored into the equation.)

Finally, the combination of the above-mentioned arguments and comparisons of each domain can conclude that it is preferable to single out a globally interconnected architecture with devices arrayed on a plane (or on planes) within a three-dimensional free-space system.

Chapter 3

Diffractive Optical Elements and Optical Interconnects

3.1 Introduction

This chapter describes a number of critical optical and optoelectronic components and techniques required for the implementation of optoelectronic neural networks for switching optimisation in Chapter 4. They include diffractive optical elements (DOEs) in Section 3.2, optical interconnection techniques in Section 3.3, vertical-cavity surface-emitting laser (VCSEL) in Section 3.4, and photodetector in Section 3.5. The case study of the Smart-Pixel Opto-Electronic Connections project is also raised in Section 3.6 before discussing about and comparing with our project in Chapter 4.

3.2 Diffractive optical elements

3.2.1 Diffractive optics

Diffractive optics is a sub-subject of micro optics. Typically a multilevel or continuous micro-relief with feature sizes range from sub-micron to millimeter dimensions. The elements in diffractive optics can be divided into two categories: holographic optical elements and synthetic diffractive optical elements (DOEs) traditionally known as computer generated holograms (CGHs). While conventional refractive and reflective elements are described by the laws of geometrical optics, DOEs are planar elements consisting of zones which retard the incident wavefront by a modulation of refractive index or surface profile and rely on diffraction to form the desired wavefront [95].

Diffractive optics is an enabling technique; the fields of its application include laser material processing, laser mode shaping, displays, advanced lithography, optical heads of optical data storage discs, and optical computing and interconnect, on which this thesis particularly discusses.

Diffractive optical elements can offer unique wavefront transformation capabilities. Their potential to provide optical computing and interconnection with fan-in and fan-out elements has been increasingly accepted and investigated. These useful optical elements have become real alternative to their refractive, reflective, and volume holographic counterparts as a consequence of recent advances and developments in

numerical design techniques and fabrication process. There are at least three reasons why the particular field of computer-generated holography has arisen. First is that novel structures can be realized, complementing and exceeding the possibilities of conventional optical components like lens, mirror, and prisms. This results from that virtually any structure shape can be fabricated and this allows all degrees of freedom in the design or control of amplitude, phase, and state of polarization. Secondly, diffractive optics and computer-generated holography emerged from conventional optical holography, but they are carried out mathematically. Third is that fabrication techniques became commercially available and appropriate for the size of these enabling elements.

3.2.2 Basic theory of Fourier-plane DOEs

Diffractive optical elements function in either the Fresnel or the Fourier domains. The difference between the two essentially relates to the distance that the light propagates, with the Fresnel-domain DOEs being used over the shorter distance. Fresnel-domain DOEs are multi-facet optical elements with each facet performing a task totally independent of neighbouring facets. On the other hand, Fourier-domain optical elements operating in the far field are particularly suited to optical array illumination and space-invariant optical interconnects as shown in Figure 3.1 (a) and (b), respectively.

The primary function of diffractive optical elements is to transform a given incident wavefront into a new diffracted wavefront. In the limits of scalar diffraction theory, diffractive optical elements is described by a transmission function $t(x, y)$

$$t(x,y) = \frac{U_{Diffraction}(x,y,0)}{U_{Incident}(x,y,-H)} \qquad \text{(Eq. 3.1)}$$

Scalar diffraction theory indicates that no polarization, multiple scattering, or volume effects are considered. It uses Fresnel or Fraunhofer diffraction integrals to propagate wavefront and implies small diffraction angles. By a diffractive optical element one refers a structured boundary region –H < z <0 between two homogeneous materials, which is designed mathematically and fabricated with the aid of a computer-controlled patterning equipment such as electron-beam lithography.

Fourier-plane diffractive optical elements are widely used in many free-space optical computing demonstrators, mainly because of their elegant feature of fanning out the incident laser beam into an array of equal-intensity, equally-spaced light spots to bias an array of logical devices as illustrated in Figure 3.1 (a) [95]. The similar type of elements can function as space-invariant interconnects as shown in Figure 3.1 (b); here illustrates a nearest neighbour interconnection. Other types of array illuminators and fan-in and fan-out elements exist including micro-lens arrays. However, these schemes share a serious drawback: the relative intensities of the light spots depend on the intensity distribution of the incident laser beam. In case of Fourier-plane elements, only the shape of each individual spot depends on the incident beam profile. Moreover, only the Fourier-type elements can be used as space-invariant interconnects in the specific geometry of figure 3.1 (b).

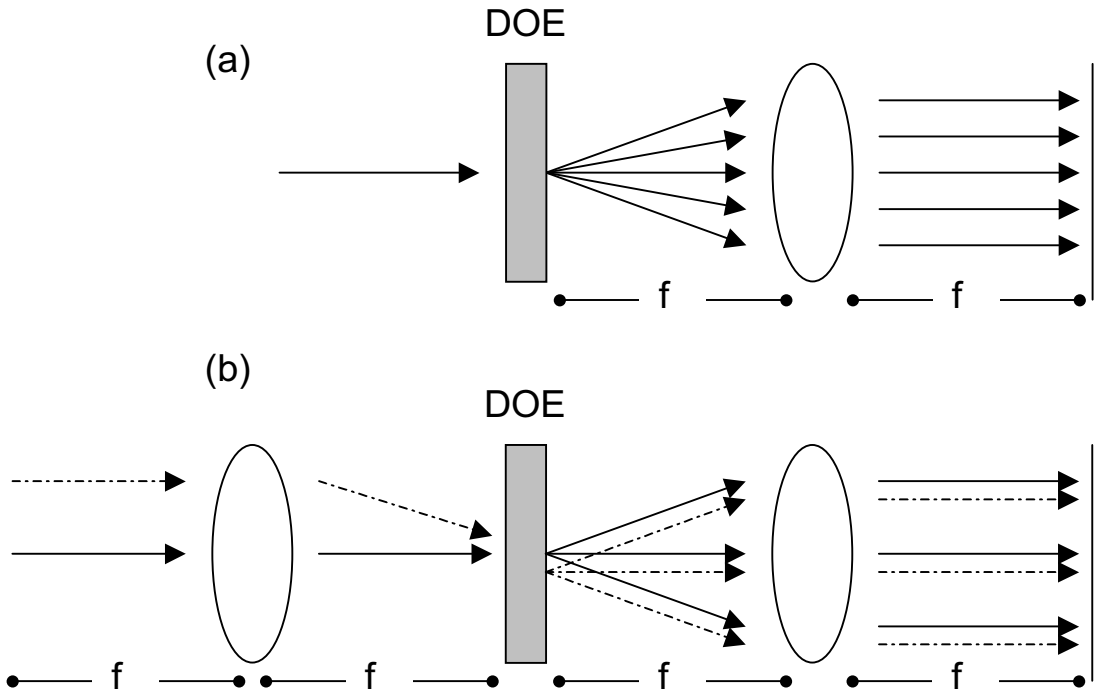


Figure 3.1 Functions of DOEs as (a) an array illuminator and (b) space-invariant optical interconnect

Due to the two-dimensional periodicity of the logic element array (period $s_x \times s_y$), the DOE must also be periodic, that is a grating with period $d_x \times d_y$. In paraxial approximation, $d_x = \lambda F/s_x$ and $d_y = \lambda F/s_y$, where F is the focal length of the lens. The field behind the DOE is $U(x,y,0) = t(x,y) \times U(x,y)$, and the field in the Fourier plane where the transverse coordinates are denoted by u and v is given by the Fraunhofer diffraction integral

$$U(u,v,2F)$$
$$= \int_{-\infty-\infty}^{+\infty+\infty} U(x,y,0) \times \exp\left(\frac{-i2\pi(ux+vy)}{\lambda F}\right) dxdy \qquad \text{(Eq. 3.2)}$$
$$= \sum_{m=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} T_{mn} \tilde{U}\left(\frac{u}{\lambda F} - \frac{m}{d_x}, \frac{u}{\lambda F} - \frac{m}{d_y}, -H\right)$$

where T_m is the Fourier-series coefficient and $\tilde{U}(f_x, f_y, -H)$ denotes the Fourier transform of the field $U(x, y, -H)$ immediately before the DOE. Assuming that $U(x, y, -H)$ represents a rotationally symmetric Gaussian beam with $1/e^2$ half-width w, the $1/e^2$ beam width in the Fourier plane is $w_F = \lambda F/\pi w$. Quantities $C_x = s_x/2w_F$ and $C_y = s_y/2w_F$, the so-called compression rations in the x and y directions, may be defined to measure spot array resolution in the Fourier plane. Existing optical logic element arrays usually require that C_x and C_y are the order of 4 - 8 to avoid power loss between the active windows. Since C_x and C_y may also be written in the form $C_x = \pi w/2d_x$ and $C_y = \pi w/2d_y$, approximately 5 - 10 grating periods must be illuminated.

When the diffraction orders of the grating are well resolved in the Fourier plane (that is C_x and $C_y > 1$), the complex amplitudes in equation determines the diffraction efficiencies

$$\eta_{mn} = |T_{mn}|^2 \qquad \text{(Eq 3.3)}$$

The efficiency of array illuminators and other Fourier-plane DOEs can be increased substantially by use of multilevel grating profiles. The design of a Fourier-plane array illuminator involves simultaneous maximization of U. Many numerical algorithms have been developed for this purpose. [95~98]

3.2.3 Fabrication of DOEs

The most common fabrication technique of diffractive optical elements is essentially micro-lithography (a semiconductor VLSI fabrication technique) with photolithography being the most prevalent. Fabrication process requires generating highly accurate binary and multilevel surface-relief profiles on suitable dielectric substrates such as glass or fused silica. For example, a transmission DOE for $\lambda = 633\mu m$ can be fabricated in SiO_2, and a reflection DOE can be fabricated in GaAs or Silicon coated with a metallic film [96]. The process involved in photolithography is schematically shown in Figure 3.2. The desired pattern is plotted in a chrome coating on a quartz substrate using an electron-beam writer. The highly accurate amplitude master mask is then replicated in a photoresist layer that coats the substrate. This is done by UV illumination of the unmasked photoresist areas in a vacuum contact copying process. Chemical development of the exposed photoresist reveals a surface profile comprising of either unexposed photoresist areas or the bare substrate material. The photoresist profile is transferred into the substrate to the appropriate depth by reaction-ion etching (RIE). As mentioned before, optical efficiency of DOEs can increase with the number of surface-relief levels. Repeating the photolithographic fabrication steps forms a multi-level surface profile. The alignment of subsequent masking layers is performed optically using a series of registration masks. In order to minimize the number of fabrication cycles with respect to the number of levels obtained, a quantised modulation with a discrete number of equally spaced phase steps, Z, is used, where Z is given by

$$Z = 2^Q \qquad \text{(Eq 3.4)}$$

and is the number of levels obtained for Q fabrication cycles. It is noted that when Z = 2 the element is referred to as a binary DOE and when Z > 2 as a multi-level DOE. Also all DOEs quantised according the above equation are commonly referred to as binary optical devices.

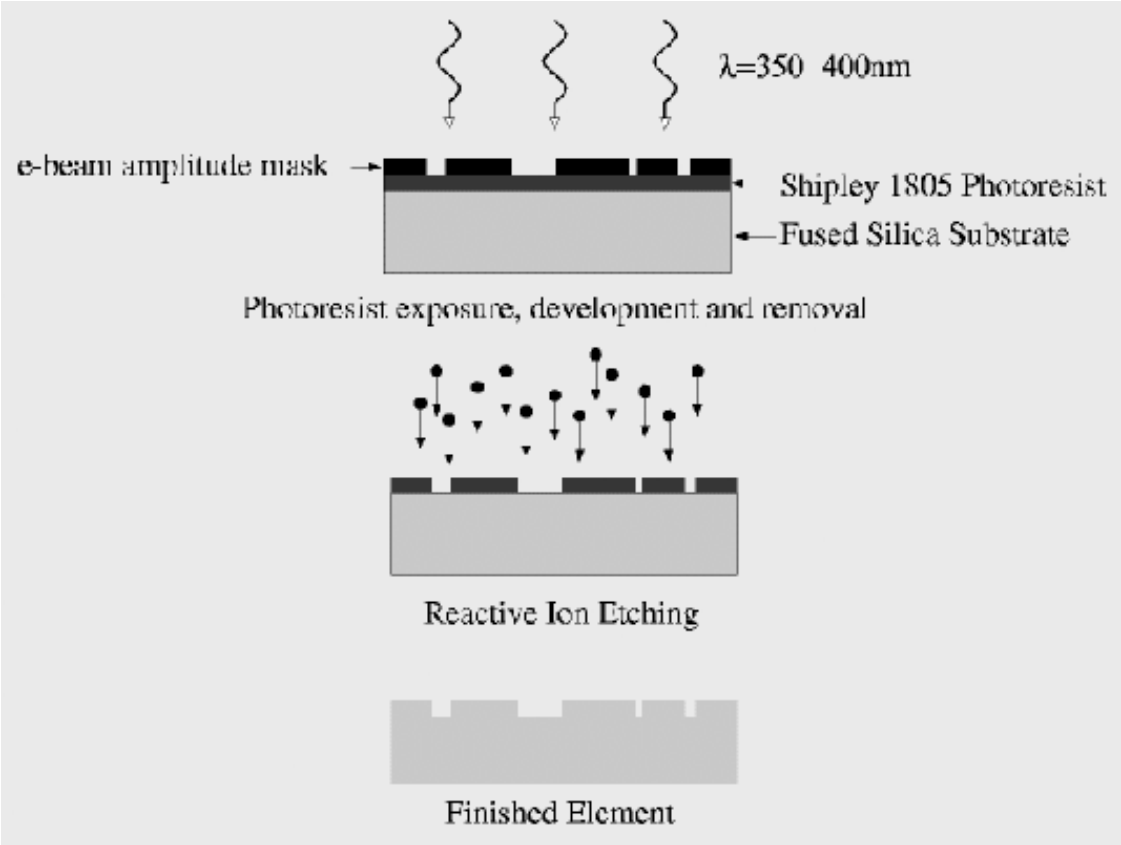


Figure 3.2 Three-stage fabrication process for fabricating DOEs. (a) photo resist exposure, and is patterned (b) and etched. (c) removing the resist layer reveals the surface profile [119].

In the scalar domain at visible and infrared wavelengths this mode of fabrication is used routinely to generate the DOE surface profiles required. Chrome master masks

can written with a resolution of 0.1 μm and feature sizes of ~ 2 μm routinely, and these features are replicated in the photoresist with approximately that resolution. At Heriot-Watt University, subsequent mask alignment is achieved to within an accuracy of ± 0.3 μm and the unmonitored etch depth controlled to within ~ 1 nm over an area of ~ 1 cm^2 or ~ 5nm in general. (See more information about fabrication at [52] [58] [61~65] [67] [68] [78] [80] [82] [92~94] [101] [103].)

Researcher in UCSD [76] reported a fabrication method using the hydrophobic effects for a polymer microlens arrays. Organic polymer microlens have been created on a lithographically patterned adhesive hydrophobic layer using dip-coating. Various lens shapes (circular, elliptical, square) have been fabricated on a variety of substrates (SiO_2, SiN, GaAs, InP, etc) ranging in size from 2 - 500μm in diameter. Plano-convex and double-convex lenses have been developed as fast as f/1.38 and f/1.2, respectively. Those microlens were directly integrated with MEMS mirror arrays as well as with the core of optical fibers. In addition, these fast conversing (small f/#) microlens arrays using this fabrication method are of particular interest in digital optical computing. Because an important challenge in the use of VCSEL arrays as input devices for free-space optical interconnects is the efficient collection of their emission.

3.3 Optical interconnects

3.3.1 Free-space optical interconnects

Optical interconnects [72] can be defined as the use of optical, optoelectronic, or photonic devices for providing interconnections in computing and communication systems with emphasis on local interconnects within a single computer or switch, rather than system-to-system local area networks [73]. Free-space optical signal transmission (as well as waveguide-based transmission) are used for optoelectronic interconnects. For both approaches, the required precision for the adjustment between the emitter array and the detector array is a major difficulty in order to realize the required sensitivity and to minimize crosstalk. Furthermore space limitations will play an important role, e.g. collimation in free space systems. For free-space interconnects, the feature of reconfigurable or dynamic interconnection schemes is of special interest, as it performs different types of functions and no electrical equivalent exists. A very higher degree of parallelism can be realized in free-space systems holding more than 10,000 (128 × 128) channels by use of DOEs in the near future. Free-space transmission obviously avoids problems that resulted from absorption and bending losses in waveguides. These connections may have a particular potential for transmission over very short distances as well as for systems with a very large number of channels. Furthermore free space systems may be particularly efficient in situations, such as one-to-many interconnects where a broadcasting distribution map of a given signal to many points on a chip are required.

The most widespread approach has been to replace the longer electrical interconnections with optical interconnections without modifying the logical architecture. Examples are optical backplanes, fixed free-space interconnections between circuit boards. In this spirit, optoelectronic technologies can be used to help wire up electronic circuits designed in the conventional way by the provision of a large number of pinouts and high-performance long-distance connections. Fortunately, the need for general conceptual analysis, simulation, comparison, and optimisation at the systems level has also been well recognized and has resulted in considerable research [87] [88] [91] [99] [100].

3.3.2 Trends in free-space optical interconnects

Free-space optical interconnects utilizing two-dimensional optoelectronic device arrays enable high-density, high-bandwidth optical communications between VLSI chips in computing systems [77]. These technologies have experienced significant progress in recent years primarily owing to the rapid advances in the areas of optoelectronic VLSI and diffractive and micro optics. Despite these achievements, a significant challenge that still impedes the successful deployment of systems is associated with the developments of cost-effective packaging and assembly techniques capable of maintaining system alignment in an industrial environment [53].

A number of different implementations are under investigation at McGill University, one of the most active research groups in this subject. Bernier, Ayliffe, and Plant at el at McGill extensively addressed the issue of alignment [53] [57]. Tolerance to misalignment was achieved through the use of two-dimensional arrays of 3 × 3

VCSELs and photodiodes together with an adaptive alignment algorithm based on redundant transceivers and a defocused optical interconnect. The system was designed to transmit four 1.25Gb/s channels and have lateral misalignment tolerance of ±1mm and angular tolerance of ±1° [90].

A compact folded structured light generator was presented by Chateauneuf at el [60]. That spot array generator used in a modulator-based free-space optical interconnect employs three cascaded diffractive optical elements which produce 4 × 8 clusters on an 800 μm × 1600 μm pitch. Each cluster is a 4 × 4 array of 13.1 μm-radius spot on a 90 μm pitch.

A collaborative group of researchers [57] in Canada and UK constructed a multi-stage free-space optical interconnection system. The system was designed to connect 4 boards in a unidirectional ring configuration for optical backplane applications. Each board is connected to an optoelectronic chip, which contains an array of 512 GaAs electro-absorption modulators and 512 photodetectors. This results in a very high density of 1250 channels/cm^2. Light is relayed between nodes with a rigid micro-optical system.

An optical circuit was built to facilitate the testing of a free-space optical interconnects based on a hybrid CMOS/GaAs chip which had a 16 × 16 array of detectors on a 250 μm pitch interlaced with a 16 × 16 array of modulators [86].

Garzia [70] at el proposed a device that is capable of switching a sequence of equally spaced pulses between two or more output, according to the switching information carried from the first pulse that behaves as an addresser. The device was proposed to act as an all-optical router and it is based on the properties of a soliton beam in a transverse refractive index profile.

3.4 Vertical-cavity surface-emitting laser (VCSEL)

3.4.1 VCSELs for optical interconnects

One of the key components in optical computing and interconnects is a light source. The most viable type of light source for inter- and intra-chip optoelectronic interconnects is vertical-cavity surface-emitting lasers (VCSEL) based on high precision epitaxial InGaAs/AlGaAs layer stacks. Key characteristics of VCSELs are low threshold currents, low-divergence, high efficiencies, compatibility with CMOS ICs for flip chip bonding integration, and compact vertical structure allowing two-dimensional integration [83] [84]. VCSEL devices may be made with other optical components and detectors in a matrix configuration and their combination opens the possibility of some interesting new devices, such as optical switching fabric. In order to focus the emitter signal, one may integrate micro-lens arrays with VCSELs.

The recent advances in VCSEL technology provide an enabling force to consider practical applications of optoelectronics in computer interconnects [83]. The technology, which allows fabrication and integration of large two-dimensional arrays of single-mode lasers, is potentially inexpensive because its fabrication process is similar to that of semiconductor chips. Once technology becomes mature, VCSELs are expected to cost about the same as other GaAs computer chips. However, it is likely that thermal management will be a problem when all lasers from a densely packed VCSEL array need to be simultaneously operated. One can see a potential advantage to optoelectronic interconnection architecture design in avoiding the requirement of simultaneous activation of a large number of VCSELs.

3.4.2 Wavelength-tuneable VCSELs

Recently a tuneable 1550nm VCSEL with a 50nm turning range has been reported [102]. The device is a micro-electromechanical structure where the top curved is displaced by a voltage-induced electrostatic force. The cavity is designed for operating under optical pumping at 980nm wavelength. The wavelength tenability allows ideal transmitters for dense wavelength division multiplexing and dramatically reduces the cost associated with allocating separate wavelengths (or channels). Such a wavelength selectable source would provide the flexibility to launch traffic on whatever wavelength is free. In fact, anywhere wavelength conversion might be done, they could help manage bandwidth and traffic in the optical domain [1].

3.4.3 Device structure of VCSELs

A VCSEL has a structure that emits a cylindrical beam perpendicularly to its p-n junction in contrast to Fabry-Perot, distributed feedback (DFB) lasers, and distributed Bragg reflector laser (DBR) lasers, whose output beam has an elliptical cross-section, typically an aspect ratio of 3:1 that does not match the cylindrical cross-section of the fiber core. Moreover they typically require substantial amounts of current to operate in the order of tens of mill amperes. Thus, a non-cylindrical beam may require additional optical components [12].

A VCSEL consists of a vertical sandwich of a p-type multi-layer, an active region, and an n-type multi-layer. The p-type and n-type multi-layers (40 to 60 quarter-wavelength layers) comprise Bragg reflectors (DBR) that are made with In + Ga + As

+ (Al or P), depending on the wavelength desired. For example, In + Ga + As + P is used for lasers in the wavelength window from 1300 nm to 1500 nm. These layers are made with epitaxial growth followed by planar processing. Cleary, the above description is very simplified; the exact process and consistency of the multi-layers and the overall device is manufacture dependent and proprietary.

The VCSEL structure is very compact and it can easily incorporate multiple quantum well (MQW) lasers, since the latter is made with the same elements and with a similar (multi-layer) structure, thus increasing the efficiency of the laser device.

An alternative to utilizing emitters as output devices is the use of modulators based on the Quantum confined Stark effect in GaAlAs/GaAs or InGaAs/GaAs quantum wells. Very large arrays of modulators (several thousands) have already been integrated with CMOS chips and operated in experimental optically interconnected systems.

Short wavelength emitters (= 0.6 μm) are attractive, because they are well matched to the attenuation spectrum of low cost PMMA based plastic optical fibers. Longer wavelength edge or surface emitters, on the other hand, are of interest because of their compatibility with long distance fiber communication. Furthermore 1.3 μm and 1.5 μm lasers have turn-on voltages below 1V, which makes them compatible to anticipated drive voltage ranges of future IC generations. VCSELs in the 0.8 μm and 1.0 μm wavelength range are available as high performance single devices as well as in small arrays. Here the main development targets address the fabrication of large two-dimensional arrays. All other material systems are at a much earlier state of development. In conjunction with plastic optical fibers, AlGaP based VCSELs or even shorter wavelength emitters based on GaN are particularly interesting. For AlGaP, AlGaSb and GaInNAs the development and optimization of electrically pumped single VCSELs will be the main target over the next years.

3.5 Photodetector

Photodetectors (or photosensors) are transducers that alter one of their characteristics when light energy impinges on them. Some photodetectors alter the flow of electrical current or the potential difference across their terminals. Some types of photodetectors with sufficiently fast response that measurable output for a small amount of light are worth investigating for applications in high-speed optical communications. These types include avalanche photodiodes (APD) and positive intrinsic negative photodiodes (PIN).

The choice of the detector and waveguide material should be governed by the operating wavelength of the emitters. InGaAs/AlGaAs, InGaAsP on InP as well as Si can be used. Silicon-based detectors, naturally, have the highest potential for monolithic integration.

However, it is arguable whether processes required for fabricating high-speed, high efficiency detectors should be consistent with the fabrication process of the IC technologies. Waveguides based on polymeric materials with losses of less than 0.1 dB/cm may offer a viable alternative for optical interconnects due to their ability to be processed at temperatures compatible with CMOS processes i.e. below 250 °C. In addition to the current workhorse systems GaAs/AlGaAs and InGaAs/AlGaAs, a number of materials are under investigation for the use in optoelectronic interconnects [12].

3.6 Case study: the Smart-Pixel Opto Electronic Connections (SPOEC) project

3.6.1 System architecture

The SPOEC project is a project dedicated to finding an optical solution to the interconnect problem and funded by the European Union under the Microelectronics Advanced Research Initiative (MEL-ARI) project. The system architecture of the SPOEC demonstrator is a packet-switched optoelectronic matrix-matrix crossbar [81] [106~109]. Sixty-four electrical signals are converted into optical signals by an electrically addressed 8 × 8 VCSEL array. Each of the 64 optical outputs from the array is fanned out 64 times by an 8 × 8 fan-out diffractive optical element (DOE). The resulting set of 4096 optical signals is relayed to a hybrid InGaAs/Si OE-VLSI chip which is partitioned into 64 blocks or "super-pixels". Each super-pixel receives the full set of 64 optical input signals and converts these into electrical signals which are electrically routed by the silicon-based 0.6 μm CMOS circuits that are flip-chip bonded to the InGaAs-based optical interface chip. The unique output from each super-pixel, which represents the one signal selected from the original set of 64, is converted back into an optical output by means of a differential pair of multiple-quantum-well modulators. So as to complete an output electronic interface, the 64 output optical signals are relayed to another hybrid chip composed of an array of photoreceivers flip-chip bonded onto a second silicon integrated circuit. The system is designed as a packet switch with the routing chip configured by the packet header. Arbitration is handled internally by means of a cyclic priority scheme. Two of the

inputs are used for the (differential) clock signals, which are distributed optically to each super-pixel.

3.6.2 Optical design and diffractive fan-out elements

The demonstrator system under construction implements a 64 x 64 optoelectronic crossbar switch as a technology test-bed. The optical layout is shown in schematic as Figure 1 below.

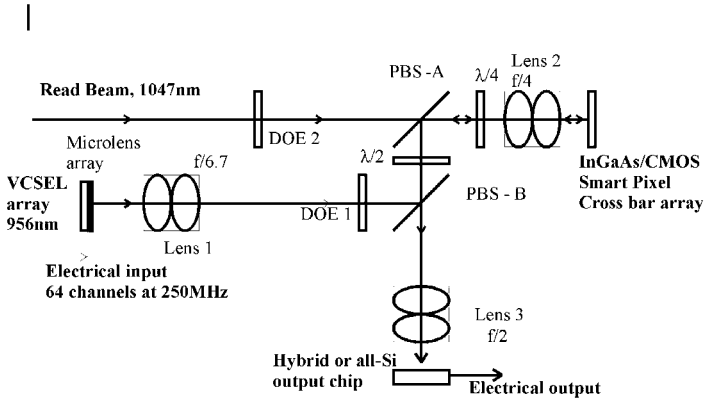


Figure 3.3 Schematic optical design layout of the SPOEC demonstrator [66]

The 64 (electrical) input data streams are converted to the optical domain by an 8 × 8 array of vertical-cavity surface emitting lasers (VCSELs) operating at 956nm wavelength. A hybrid micro-lens and bulk lens combination collect the emission and collimate it before it is fanned out 8 × 8 times using a diffractive optical element (DOE 1). The fanned out signals are routed to a hybrid OE-VLSI chip by thin-film beam-steering elements (PBS-A and PBS-B) and an imaging lens (Lens 2). The fan-out results in an 8 × 8 array of identical images of the input VCSEL array falling on the hybrid InGaAs/CMOS OE-VLSI smart-pixel crossbar array chip [89]. The 64-

times fan-out combined with the 250Mbit/s/channel data rate corresponds to an aggregate 1 Tbit/s i/o to this switching chip. The silicon circuitry of the chip implements header-decoding and routing of the data to differential output modulator pairs which are read by a 1047nm wavelength Nd:YLF laser and the reflected data streams are routed using polarisation control to a second hybrid OE-VLSI chip which converts the output data back to the electrical domain. The compact (30cm × 20cm × 10cm) system will be mounted on a slotted baseplate using custom optomechanics to give the required stability.

3.6.3 VCSEL and microlens array

The electrical inputs to the demonstrator are converted to optical signals by an 8x8 array of top-emitting MOVPE-grown VCSELs [107]. These consist of 30.5 pairs of λ/4 thick $Al_{0.9}Ga_{0.1}As$ and GaAs layers for the bottom Bragg mirror and 22 pairs for the top mirror. The cavity is 270 nm long including three 8 nm wide $In_{0.13}Ga_{0.87}As$ quantum wells separated by 10 nm wide GaAs barriers. A λ/2 thick GaAs contact layer concludes the structure. The 10 μm diameter VCSELs are on a pitch of 250 μm. The measured capacitances of the centre VCSEL (longest wiring) and border VCSEL (shortest wiring) are 3.05 pF and 1.05 pF, respectively.

The DC electrical and optical characteristics of the VCSEL array bonded onto their PCB are as follows: mean threshold current 2.6±0.05 mA, mean threshold voltage 1.90±0.01 V and output power (at 8 mA) 1.25±0.02 mW. Fully operational arrays have been fabricated with an emission wavelength of 956 nm and ±0.7 nm variation at 8 mA current. High frequency operation of the VCSEL array, prebiased at 1.9 V

threshold, has been successfully tested with data rates up to 500 MBit/s. Electrical crosstalk has been measured to be below 10%, which was shown to originate from the parallel wiring on the PCB.

The VCSEL array is mounted on a sapphire substrate, on a custom-designed PCB. The VCSEL was modelled as a 105 Ω resistance at the current-voltage operating points (2.6 mA, 1.85 V) and (8.0 mA, 2.44 V). Using this model, a passive impedance two-port network has been designed to match the 50Ω driver and the VCSEL load. This gives a compromise between maximum bandwidth and a minimum sensitivity to the variation in the VSCEL characteristics over the array. For 0 and 1 having the same probability of appearing in the data, the heat dissipation is 0.77 W for the VCSEL array and 6.14 W for the PCB. A temperature sensor and Peltier element are included for temperature control.

An important challenge in the use of VCSEL arrays as input devices for free-space optical interconnects is the efficient collection of their emission. This is particularly important in a system such as this, where 64 VCSELs are fanned out to 4096 detectors. To maximise the optical power reaching the detectors we have integrated a refractive microlens array (8×8 f/5 lenses operating at f/3) to collect 90% of the emission and reduce its divergence to match the f/6.7 bulk Lens 1. This combination allows efficient collection while retaining the necessary illumination of multiple periods of the diffractive element DOE 1 for efficient fan-out. The packaging scheme is shown in Figure 3.4. A mounting ring around the VCSEL array provides the correct stand-off with lateral alignment provided in manufacture by the reflection of an alignment

laser from diffractive zone-plate lenses included in the corners of the VCSEL array metalisation [66].

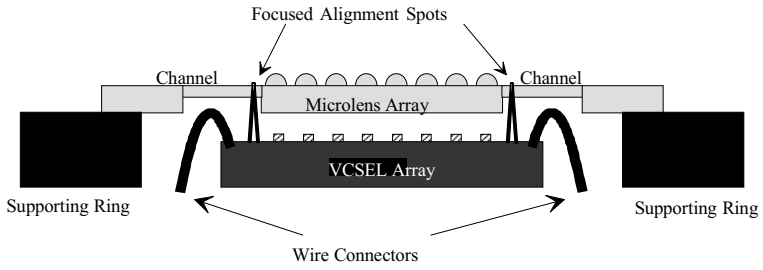


Figure 3.4 Hybrid mounting scheme for a microlens array on a VCSEL array [66]

The 8 × 8 fan-out of the VCSEL emission and the generation of the 8 × 16 array of read-out beams from the Nd:YLF laser will be performed by binary phase-only diffractive optical elements. Whilst both binary and 8-level elements have been manufactured, initial system testing will use the binary designs, preferred because of their more effective zero-order suppression to ~0.05% (to reduce crosstalk) and low (1-3%) non-uniformity although at some cost in reduced (~60-65%) diffraction efficiency.

3.6.4 InGaAs Modulator and detector

The III-V semiconductor optoelectronic interface arrays consist of differential modulator pairs and single-ended detectors. The two diodes in the differential output pair use a common n-type bias voltage and separate digital driver circuits are used to drive the two p-type contacts with the true and complementary data. Compared to the

conventional approach of two series-connected modulator diodes, this approach reduces switching noise on the modulator bias voltage, but requires larger silicon driver circuits to sink the total photocurrent through each diode of the pair rather than the difference between the two. The modulator bias voltage is separated from the detector bias to avoid electrical crosstalk and to permit separate optimisation.

The arrays are fabricated from In(Al,Ga)As strain-balanced multiple quantum well (MQW) p-i-n structures grown by molecular beam epitaxy (MBE). The structures are deposited on GaAs substrates with an intervening buffer layer 2μm thick containing a linear grade in In concentration. The top p^+-InGaAs contact layer includes Be δ-doping to facilitate the formation of low resistance, non-alloyed ohmic contacts. Fuller details of the MBE grown MQW layers have been described in []. The processing of the arrays includes (1) mesa isolation of the individual devices by a two-step wet chemical etch; (2) lift-off of a sputtered gold film with a bi-layer photoresist to form non-alloyed contacts to the detectors and modulators (the gold film serves the additional purpose of a high reflectivity mirror); (3) trench isolation of the lower n^+ contact layer to disconnect electrically the modulators and detectors, and (4) overall passivation with PECVD SiO_2. Test diodes indicate turn-on voltages ~ 0.8 V and reverse saturation currents of <10 nA for a mesa with a diameter of ~35 μm. The modulators used in the demonstrator system are designed to operate with the available 5 V. There is a clear trend to decreasing voltages being used in the underlying silicon CMOS. Thus modulator design at lower voltages is an important issue, as is improved modulator performance at the present 5 V bias. The incorporation of an optical cavity in the design is being pursued to address these questions, with encouraging results [59] [107].

3.6.5 Summary

The system design is intended to demonstrate the technological potential of OE-VLSI in the terabit/s regime without addressing any particular application area. It designed and built a hybrid system with 4096 optical inputs to a single CMOS chip with each input carrying data at up to 250 Mbit/s. All the tests show that the system is working to the desired specification. Full operation of the test bed, with all 4096 channels working simultaneously, will correspond to an aggregate input of more than 1 Tbit/s [4].

Chapter 4

Implementation of Optoelectronic Neural Networks for Switching Optimisation

4.1. Introduction

4.1.1 Overview of the demonstrator

The new demonstrator has been designed to perform as optoelectronic neural networks for switching optimisation. The demonstrator consists of the optical and electronic subsystems. The optical subsystems holding an 8 × 8 array of vertical-cavity surface-emitting lasers, photodiode detectors, and a pair of lens and a diffractive

optical element has been mounted on an optomechanically-designed baseplate. The electronic subsystem employs digital signal processors (DSPs), and analogue/digital converters for representing neurons of Hopfield neural networks. In this implementation, both a crossbar switching fabric and a multistage self-routing switch fabric were considered.

This chapter shall report on the design and progress of each component of the optical and electronic subsystems and the system implementation of optoelectronic neural networks for switching optimisation. Section 4.1 gives a brief description of crossbar switch fabric and self-routing switch fabric. The progresses in the optical and electronic subsystems are mentioned in Section 4.2 and Section 4.3, respectively. Section 4.4 investigates about the scalability of the neural networks and describes about the system construction and comparison with the SPOEC demonstrator

4.1.2 Crossbar switch fabric

This subsection considers specifically the assignment problem in a crossbar switch for packet routing. In the case of a crossbar, the neurons correspond directly to the cross points of the switch. The neuron outputs can vary continuously between the off and on levels. In order to choose a set of connections, the neurons representing all the requested connections are enabled simultaneously and set to the same intermediate level. Each has a bias input that tends to increase its output, but also receives inhibitory inputs from those neurons which represent blocking connections.

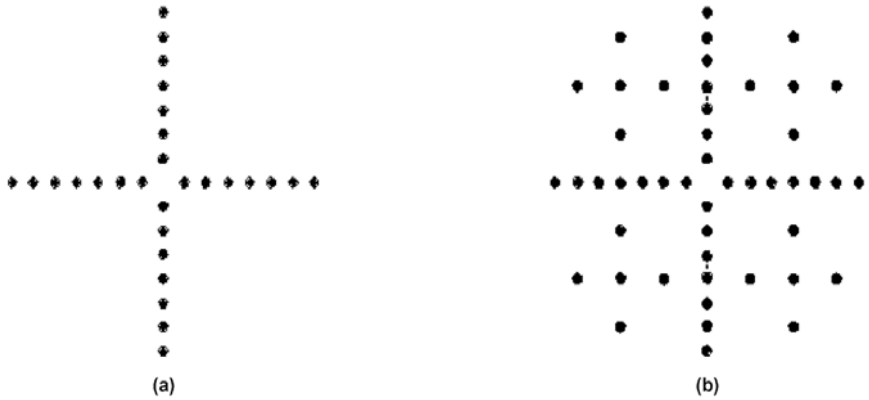


Figure 4.1: Inhibitory DOE interconnection patterns. (a) illustrates that for a crossbar switch, (b) for a self-routing network. All spots indicate an inhibitory interconnect.

Crossbar switches can be blocked at their inputs and outputs only, so the neurons are arranged to be inhibited by others in the same row or column [116].

4.1.3 Self-routing switch fabric

Other types of switch can be blocked internally, for these switches additional inhibitory connections are provided between the appropriate pairs of neurons. The dynamics of the network resolve the conflicts between all the mutually exclusive neuron pairs, leaving a valid set of neurons in the on state and the remainder off. The network is thus behaving as a winner take all (WTA [124]) system with a particularly simple interconnect pattern – each neuron sees only its row and column neighbours, each of which are connected to it by a fixed inhibitory weight. Sample interconnect patterns are shown in figure 4.1 [116].

In this implementation, each of the 48 neurons (6×8) has an input detector followed by a capacitor-coupled inverting amplifier chain and a low-pass filter, and the output drives a VCSEL. Initially all the lasers are set to a fixed output level, slightly higher than the off level. This sets a stable total power for the array and effectively biases the neurons towards the on state. When the network is enabled, the lasers of all the requested neurons are connected to their amplifier outputs and the others are set to the off level. Between the laser and detector arrays are a pair of lenses and a DOE that divide the light from one neuron's laser and focus it onto the inputs of the other neurons in the same row and column, but not its own input. Due to inversion in the amplifier chain, light falling on a detector inhibits the associated neuron, decreasing its output [124].

4.2. Optical Subsystems

4.2.1 Optical set-up

The optical subsystem of the neural network hardware constitutes interconnections between the neurons by means of a combination of diffractive optical element (DOE) and a single lens. The schematic layout of the optical set-up is shown in Figure 4.2. This simple optical architecture allows maximum flexibility of interconnection pattern as inserting a different design of a DOE into the system can change the interconnection pattern.

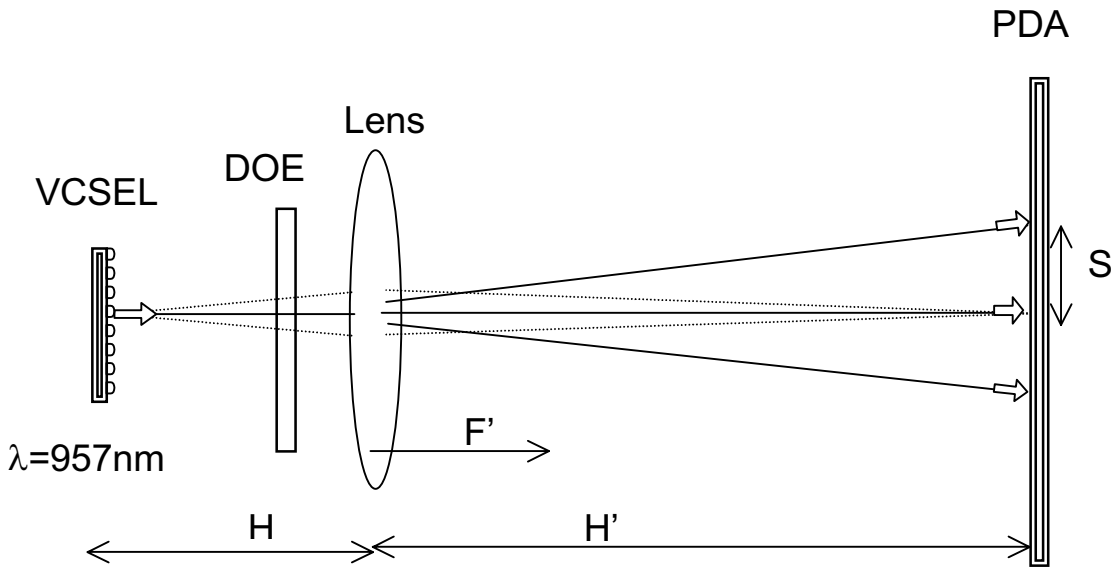


Figure 4.2 Schematic layout of optical set-up

The neurons themselves are implemented electronically using a number of Digital Signal Processors and is discussed in Section 4.4. The electronic-optic conversion is performed by a two-dimensional (8×8) array of VCSELs, operating at wavelength λ= 960nm, and a two-dimensional (8×8) array of Si photodetectors is used to convert the optical signals back to electronic signals. The entire optical subsystem, which includes the optomechanical and optoelectronic subsystems, is shown in Figure 4.3 with the optical signals propagating from right to left.

$$Magnification = \frac{PDA(spacing)}{VCSEL(spacing)} = \frac{1500\mu m}{250\mu m} = 6 \quad \text{(Eq. 4.1)}$$

$$\begin{cases} h' = 6 \cdot h \\ \frac{1}{h} + \frac{1}{h'} = \frac{1}{f'} \end{cases} \quad \text{(Eq. 4.2)}$$

The lens used in this assembly was chosen to generate the necessary ×6 magnification to match the spacing of VCSELs (250μm) to that of photodetectors (1.5mm). According to Equations 4.1 and 4.2, the total distance (h + h') between the VCSEL and photodetector arrays was calculated to 163mm in using a lens with the focal length of 20mm.

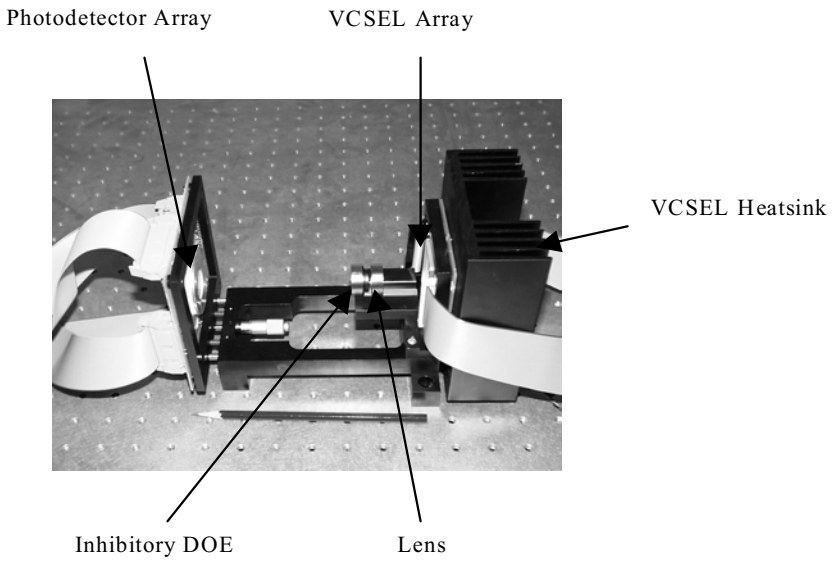


Figure 4.3: Optical Subsystem mounted within optomechanical baseplate

4.2.2 VCSEL array

The VCSEL array used in this experiment was supplied by CSEM and it photograph is shown in Figure 4.4 [119]. The diameter of each output is 10 μm and the spacing between VCSELs is 250 μm. The mean threshold current I_{th} is 2.57 ± 0.05mA; the mean threshold voltage V_{th}, 1.95 ± 0.01V; the mean optical output power (at 8mA) P_{VCSEL}, 1.25 ± 0.02mW. The operating emission wavelength λ is 957nm with a maximum variation $\Delta\lambda$ of 0.25nm [49].

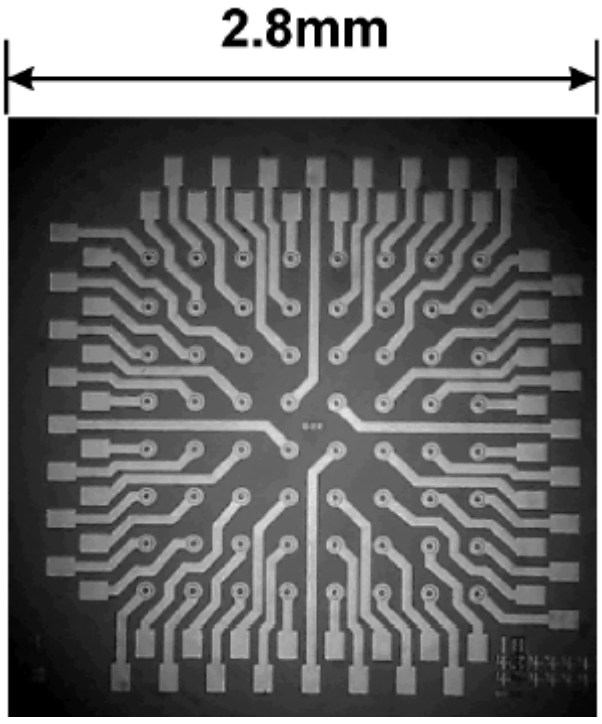


Figure 4.4 Photograph of an 8 × 8 VCSEL array produced in CSEM

Each illumination of a single VCSEL represents the output of a neuron, which forms the inhibitory interconnections between the neurons in the Hopfield neural network.

Each VCSEL beam form a Gaussian shape with an 8° divergence. After projection through the optical elements, the average beam diameter is 64.7μm compared to a diffraction limited spot size for the optical system of 34 μm.

4.2.3 Diffractive fan-out optical elements

The diffractive optical element was designed using a combination of an iterative Fourier transform algorithm (IFTA) [125] and a closed-form trapezoidal algorithm. In general, these standard design methods allow the creation of DOEs with efficiencies of > 70% and reconstruction errors of < 1%. However, due to the restrictions placed upon the DOE period by the optical system described above, a reduction in the overall efficiency of the DOE to 50% was required to ensure that the reconstruction error was of an acceptable level. The period of the DOE is given by

$$T = \frac{nf\lambda}{s} \quad \text{(Eq. 4.3)}$$

where n is the number of orders between co-linear "on" diffraction orders, f and λ are the focal length and wavelength respectively; s is the separation between "on" diffraction orders. Figure 4.1 shows the output from two different inhibition DOEs, the first was designed with the co-linear spacing between the "on" diffraction orders set at one diffraction order and the second with the co-linear spacing set to two diffraction orders.

It has be concluded that the larger period produced by the double order spacing has improved the overall uniformity of the element. This improvement in final uniformity

is due to the larger minimum feature size of the double order spacing element and the commensurate improvement in the photolithographic transfer of the phase profile onto the glass substrate.

4.2.4 Photodetector array

The 10 × 10 photodetector array used in this experiment is shown in Figure 4.5 and support a relatively high data rate, as its typical response time is 26ns. The function of this photodetector is to convert the optical signals back to voltage in conjunction with a trans-impedance amplifier. The size of each photodetector element is 1.4m × 1.4m; the pitch between elements is 1.5mm; the responsibility at the operating wavelength (λ = 957nm) is 0.33 [49] [119].

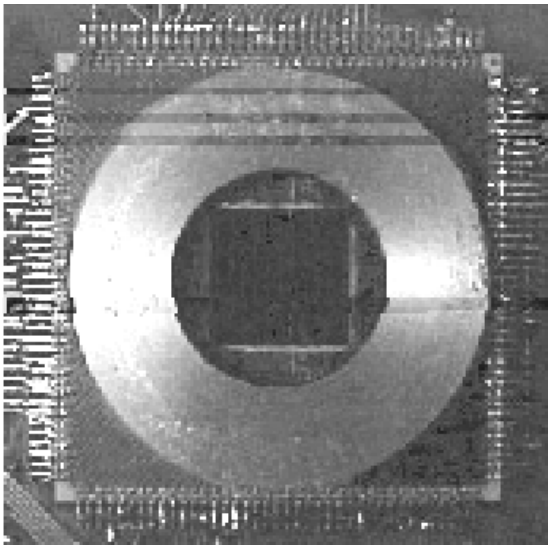


Figure 4.5 Photograph of an 10 × 10 Si photodetector array produced by Centronic

4.2.5 Optomechanical design and thermal consideration

The optomechanical baseplate (whose CAD design is shown in Figure 4.6) facilitates the focus adjustment of the VCSEL array with the photodetector array as well as allowing the relative longitudinal positions of the lens and DOE to be altered without changing their transverse positions. This complete packaging scheme achieves mechanical and thermal stability.

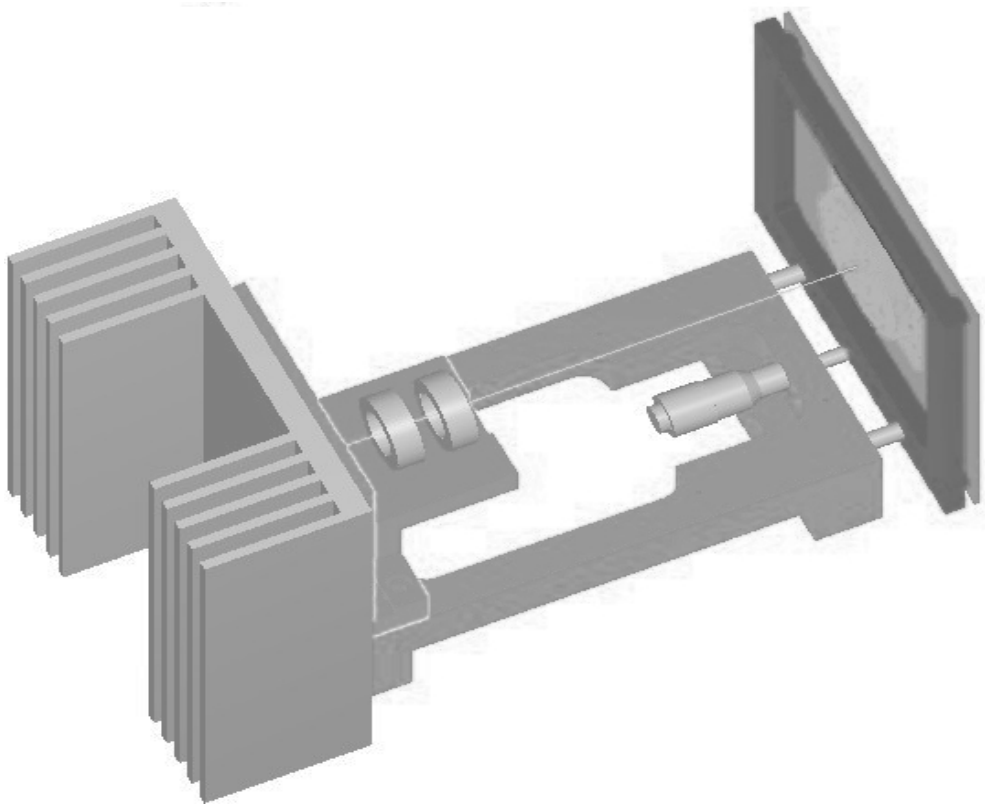


Figure 4.6 Computer-aided design of optomechanically designed baseplate

A heat sink was attached with the VCSEL array and PCB in order to keep these components as thermally stable as possible and to avoid large variation of the emission wavelength of VCSELs owing to temperature difference. Specification of the heat sink requires thermal resistance *R*. Thermal resistance is a measurement of

the difference in temperature between the component and the heat sink. This difference was intended to be as small as possible so that the heat sink can release heat from the component effectively. The thermal difference is defined by

$$R = \frac{\Delta T(C^o)}{P(W)} \qquad \text{(Eq. 4.4)}$$

where ΔT is the allowable difference in temperature and P is the total heat dissipation generated by the VCSEL array and PCB. The results of the SPOEC demonstrator indicated that the reasonable temperature difference was 10C° and that the total heat dissipation was about 7.0W (0.77W for the VCSEL array and 6.14W for the PCB) [107]. Assuming that this implementation involve with similar values of temperature difference and heat dissipation, the desired thermal resistance is expected to be less than 1.4 C°/W. Taking into account that any unexpected additional thermal dissipation can happen, a heat sink with thermal resistance of 0.5 C°/W was attached.

(See more information about optomechanical design at [111~113] [126]

4.3. Electronic Subsystems

4.3.1 Amplifier, DSP, ADC, DAC

The electronic subsystem of the neural demonstrator consists of five stages, each performing a specific task as shown in Figure 4.7 [116] [117].

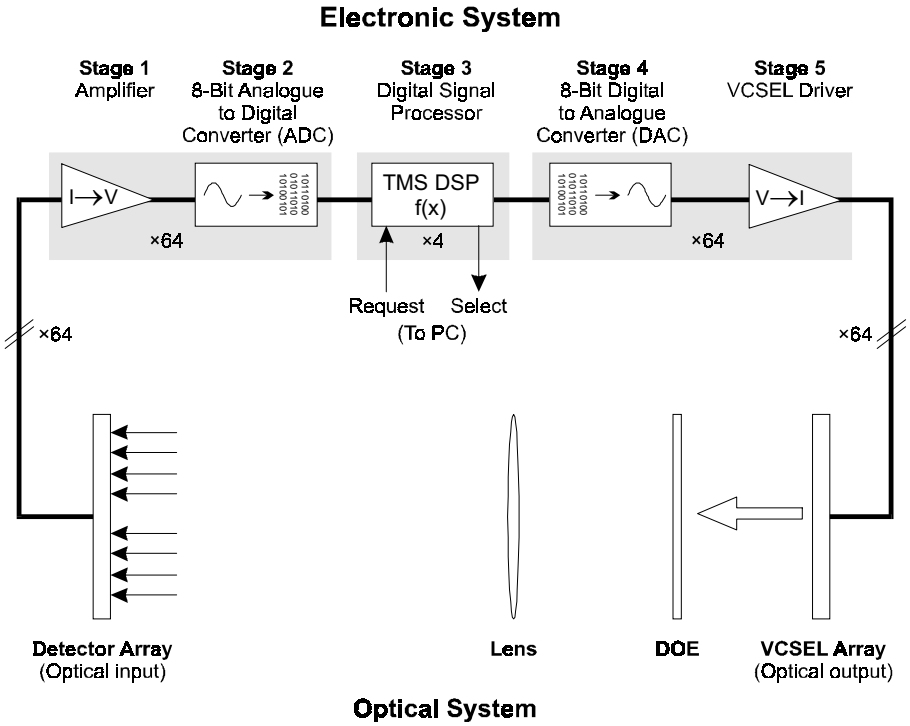


Figure 4.7: Components of electronic and optical subsystems

Starting at the optical input there is a detection system that converts the photocurrents generated by the photodetector array in to voltages. These voltages are passed through 8-bit analogue-to-digital converters (ADCs) and the converted signals are time-multiplexed onto the Digital Signal Processors, which comprise the next stage. This stage consists of 4 Texas Instruments TMS320C5X DSPs that take the digital information from the ADCs and performs the dynamic update and transfer functions specified earlier. The fourth stage converts the digital values generated by the DSPs back into analogue voltages, using 8-bit digital-to-analogue converters, for delivery to the final stage that is the driver circuitry for the vertical-cavity surface-emitting lasers. The use of commercially available DSPs to implement the neural threshold functions exhibits multi-functionality of the neural network to be altered and new problems to be tackled with minimal alteration of electronic and optoelectronic hardware.

Currently, there are four DSPs operating in a time-multiplexed manner where each DSP handles 16 inputs and 16 outputs in a single network cycle. The DSPs act as slaves to a master CPU, in this case a PC, which can be used to reprogram the DSPs [116][119].

4.3.2 VCSEL driver circuits

Two different VCSEL driver circuits were designed, the first using discrete digital components to provide the necessary drive current and the second a custom-designed application specific integrated circuit (ASIC) fabricated through the MOSIS brokerage service. Some output voltage swing of the photodetector driver circuit was observed in the far-field output of the inhibitory interconnection DOE under the circumstance of illumination from a single VCSEL modulated at 5kHz.

The modulation frequency is significantly below the theoretical maximum modulation frequency of both driver circuits (100 MHz for the digital driver and 10 MHz for the analogue driver) and it was chosen to allow the data acquisition card used in the experimental system to accurately measure the voltage. The experimental digital driver was modulated using a TTL (0-5V) square wave and the simulated analogue driver was driven using a 1V-2V sinusoidal wave, both being sufficient to produce enough current to switch the VCSEL between no optical output and an optical output of ~1mW. The total amount of optical power incident upon a single photodetector from one VCSEL has been calculated by

$$P_{\text{sin}gle\_\text{det}ector} = \eta_{bulk\_optics} \frac{\eta_{DOE}}{4(N-1)} \times P_{VCSEL} \qquad \text{(Eq. 4.5)}$$

where P_{VCSEL} is the optical power of one VCSEL; N, the size of the neural network; the efficiency of bulk optics; η_{DOE}, the efficiency of a DOE.

In the demonstrator ($N=8$, $\eta_{bulk\_optics} = 0.95$, $_{DOE} = 0.5$ and $P_{VCSEL} = 1mW$), the optical power on a single photodetector is calculated to ~17mW. The observed voltage swing of 60mV (corresponding to an optoelectronic amplification of 3500) for a single incident VCSEL beam implies that the total voltage swing for a photodetector with the maximum number (14) of optical inputs incident upon it will be ~1V.

Figure 4.8 shows the fabricated analogue VCSEL driver, which is currently being tested and will replace the digital driver circuit in the completed demonstrator system [119].

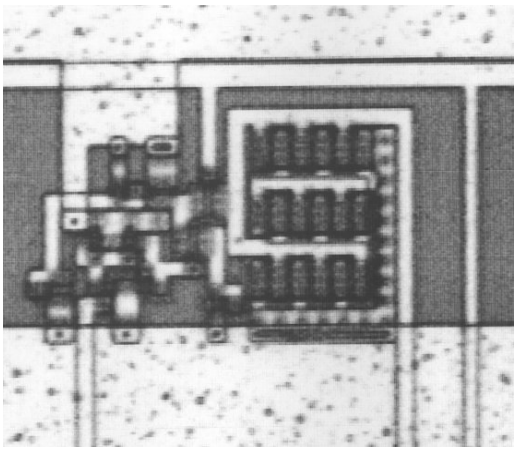


Figure 4.8 Micrograph of analogue VCSEL driver circuit

fabricated using a 2μm 2-poly 2 metal CMOS process

4.4. System Implementation

4.4.1 Scalability consideration

In principle, the Hopfield network architecture discussed in this thesis is highly scalable with the maximum size of network being set, at present, by the size of available two-dimensional arrays of VCSELs and photodetectors. However, in practice a more fundamental limitation on the maximum size of network is imposed by the non-uniformity of the diffractive optical element. This quantity, also known as the reconstruction error, is a measure of the divergence of the observed far-field diffraction pattern from the ideal pattern used in the optimisation of the phase profile. This is expressed mathematically as,

$$\Delta r = \max_{m,n \in M} 1 - \frac{I_{mn}^{\text{observed}}}{I_{mn}^{\text{target}}} \qquad \text{(Eq. 4.6)}$$

where M is the set of diffraction orders used to specify the far-field output of the phase element. Typically, the non-uniformity of binary (2 level) phase elements is of the order of 0.1% after the design process and 1-2% after fabrication. The observed increase in non-uniformity after fabrication is due to inaccuracies in the etching of the glass substrate as well as poor photolithographic transfer of fine (high spatial frequency) features from the e-beam written mask to the glass substrate. Figure 4.9 shows a section of a grating with minimum feature sizes of ~1.5 μm which is the limit

of the in-house DOE fabrication facilities at Heriot-Watt University. The sharp features of the ideal phase profile have become rounded and some of the finest features have disappeared.

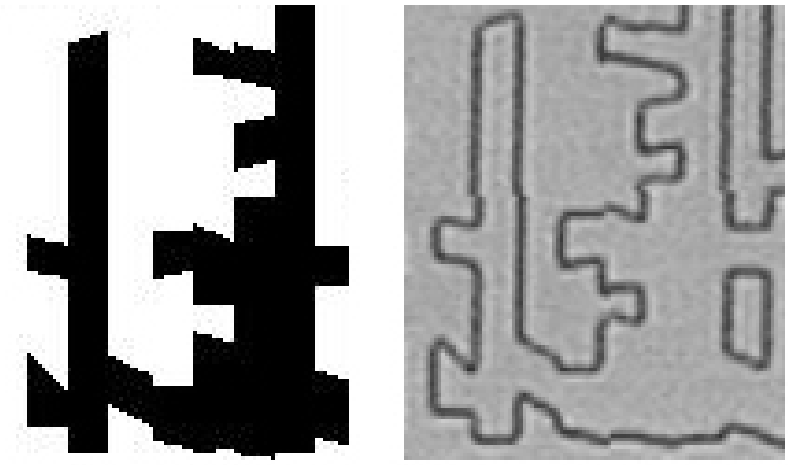


Figure 4.9: Section of inhibition pattern DOE showing photolithographic blurring of sharp features

In order to quantify the effect of DOE non-uniformity on the optoelectronic Hopfield network a simulation of the system was implemented with a non-uniform inhibition interconnection. By varying the total non-uniformity of this interconnection and observing the acceptance ratio, defined here as the proportion of test cycles where the optimal number of data channels are routed through the crossbar switch, an estimate of the limitation on network size due to interconnection non-uniformity can be derived. The optimal number of data channels that can be routed through an $N \times N$ crossbar switch is N. It can be shown the variation of acceptance ratio with increasing levels of interconnection non-uniformity for three different Hopfield network sizes. In

each case 10000 cycles of the network were analysed and it was observed that when the network was operating correctly, the acceptance ratio was above 99%.

Simulations [119] have shown that as the size of the network increases the maximum tolerable non-uniformity decreases. These simulations were repeated for a range of different network sizes and their corresponding maximum non-uniformities. They are sampled in Table 4.1.

Network size	Maximum interconnection Non-uniformity
2 × 2	19.45 %
4 × 4	8.53 %
8 × 8	4.02 %
16 × 16	1.95 %
32 × 32	0.96 %

Table 4.1 Samples of network sizes and their corresponding maximum tolerable interconnection non-uniformity

The maximum interconnection non-uniformity for an N × N Hopfield network was simulated according to

$$\Delta r_{\max}(\%) = \frac{100}{C_1 \times N + C_2} \qquad \text{(Eq. 4.7)}$$

where C_1=3.288 and C_2= − 1.435.

By assuming that the minimum interconnection non-uniformity of any DOE is 2 % and solving the above equation, the maximum size of Hopfield network which can be implemented using the current DOE fabrication technology is approximately 16 × 16. By changing the optical subsystem to allow a larger DOE period the minimum non-uniformity can be reduced, provided care is taken to remove excessively sharp features from the phase profile during the design phase. In addition, further improvements in the photolithographic techniques used in the fabrication of diffractive optical elements will achieve finer features and will again reduce the minimum non-uniformity to 1%. A combination of these methods will increase in the maximum size of Hopfield network up to 30 × 30 unless one encounters unavoidable errors in the fabrication process (e.g. in the etch depth) [119].

4.4.2 Comparison with The SPOEC demonstrator

Table 4.2 summarises the simplified comparison between the SPOEC demonstrator described in Section 3.6 and the newly implemented demonstrator presented in this chapter.

	SPOEC	This project
Optical lens design	Multi-element lenses	Single camera lens
Imaging	4-f imaging	"2-f" imaging
Hardware scalability	Difficult	Relatively easy
Fan-out elements	Space-invariant	Shift-invariant
Components	Mostly custom-designed	Mostly commercially available

Alignment	Highly challenging	Relatively easy (due to bigger spacing of detectors)
Size of baseplate	$20 \times 10 \times 30$ cm^3	$12 \times 15 \times 25$ cm^3 (25% off SPOEC)
Interconnect density	High density (< 4096 connections)	Relatively high density
Channel rate	250 MHz (500MHz tested)	10 MHz (analogue) 100 MHz (digital)
Aggregate throughput	Expected up to 1 Tbit/s	Yet to be examined

Table 4.2: Different characteristics of the SPOEC demonstrator and this demonstrator

4.4.3 System construction

All the components of the optical subsystem that contains vertical-cavity surface-emitting lasers, photodiode detectors, and a diffractive optical element have been mounted on an optomechanically-designed baseplate. It highlighted the packaging scheme facilitating focus adjustments and mechanical and thermal stability by considering the thermal resistance. This free-space optical interconnection architecture exhibited high interconnection density. The scalability of the neural networks was analysed by consideration of non-uniformity of diffractive optical elements. It has been shown that the optical subsystem can generate two different interconnection

patterns and perform two different functions with minimal realignments of diffractive fan-out optical elements.

The assembly and characterisation of the optical and electronic subsystem have been completed. The optomechanical package accommodates all the optical components within a miniature space of approximately 12cm×15cm×25cm.

Chapter 5

Conclusions

5.1 Further work

Topics in which further work is desirable in this specific implementation can be identified in a number of areas; further developments of DSPs to perform the neural threshold functions towards a full system operation are required. Integrating of VCSELs with a microlens array for efficient collection of the VCSEL emission should be at least worth considering. As shown in simulations, employing of larger arrays of VCSELs and photodetectors (for example, 16 × 16 or 32 × 32) will be highly prospective to implement and will provide a good chance to justify the simulations on the scalability of Hopfield neural networks. Previous works indicated that successful deployments of systems were often associated with alignment problems in the course of operation. Due to a relatively big spacing of the photodetectors, the likelihood of significant alignment problems is not high but care should be made.

In addition to crossbar and self-routing switches, a relatively new category of problems to be tackled by free-space optical interconnects is found in the area of optical channel cross-connects, a key function in optical networking. The cross-connecting fabric is capable of interconnecting thousands of inputs with thousands of outputs. It is desirable that the implementation of optical cross-connects should be investigated in hybrid (optoelectronic) approach or all-optical approach by use of some existing expertise obtained from this work in switching problems.

5.2 Conclusion

This thesis embodied a critical review of the field of free-space optical interconnects together with new proposals and new results of a novel optoelectronic architecture for the prototype. This work has considered the problems in switching optimisation by use of optoelectronic neural networks. The work featured in this thesis has significance in two areas.

Firstly, this work has made and reasoned a decision in the architectural choice for optical interconnections according to the interconnection theory. In the case of the prototype, it achieved a globally interconnected free-space optical architecture with devices arrayed on parallel planes in a three-dimensional system by incorporating DOEs, VCSELs, and photodetectors. However, in general, the choice between different architectures often highlights a trade-off, such as cost, performance, and alignment difficulty. Therefore, the decision of which type of architectural choice should be made is still widely open and should be finalised only once the overall experimental prototype is fully operational.

Secondly, this work has incorporated a detailed investigation and the progress of key components and subsystems of the prototype system. The assembly of the optical and electronic subsystems and characterisation of the individual components were completed and validated. Although full experimental tests on the prototype system are yet to be performed, the completion of the full system architecture has already highlighted several superior features of this optoelectronic architecture:

1) It exhibited the dual functionality of optimising two switching fabrics with minimal realignments of DOEs and programmability of DSPs.

2) The optomechanically-designed baseplate together with a heat sink facilitated the mechanical and thermal stability.

3) Simulations have shown the scalability of neural networks up to approximately 30×30.

4) The implementation emphasised the commercial availability and reliability of most components (photodetectors, lens, DSPs, ADC, DAC, etc.).

5) The optomechanical package achieved accommodating all the optical components within a miniature space of approximately $12\times15\times25 cm^3$.

Successful operation of the entire system, if achieved, would clearly be of much greater significance. Although a small number of steps need to be completed to achieve full system operation, an important characteristic of the system is that partial failures of the commercially reliable individual components are unlikely to cause a fatal failure of the entire system. Irrespectively of whether a successful operation is achieved, there is no doubt that the obtained results will be an excellent guidepost to construct both experimental prototypes and commercially practical systems of

massively parallel free-space optical interconnects for switching and cross-connecting in the foreseeable future.

Chapter 6

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