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Wideband transconductance-transimpedance post-amplifier for large photoreceiver arrays

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A photoreceiver post-amplifier circuit based on a transconductance-transimpedance cascade id presented which meets the specific performance requirements of dense photoreceiver arrays comprising hundreds of high bit rate channels. Simulations of 1Gbit/s receivers show an improvement in sensitivity, at some cost in layout area, over previous circuits based on low-gain voltage amplifiers.

Introduction: Parallel optical interconnects are being considered as a method of providing terabit/s interfaces to future generation VLSI circuits [1, 2]. To implement optoelectronic interfaces supporting these data rates, each chip requires many hundreds of high bit rate photoreceivers. Thus, to be viable for this application, a particular photoreceiver circuit must be compact and have low power; these requirements are different from those of a stand-alone telecommunications receiver where very high sensitivity is the priority.

The transconductance-transimpedance cascade has previously been applied to high frequency amplifier circuits [3] including stand-alone optical receivers [4]. Here, we propose the use of this technique for receiver post-amplifiers in large arrays. We demonstrate that it has characteristics which are compatible with the requirements of such an application and discuss how it might be preferred to existing approaches. We focus on photoreceivers with a two-beam optical input implemented in a technology employing flip-chip integration of large arrays of optoelectronic devices (such as photodiodes and MQW modulators) with foundry VLSI circuits.

A common approach for this application is shown in Fig. 1 [5]. A differential photocurrent is converted to a voltage using a simple transimpedance front-end A. The post amplifier B consists of an inverter, matched to the front-end, with a diode-connected load that is used to trade off the gain of an unloaded inverter for increased small-signal bandwidth. A final limiting stage C produces a fully restored output suitable for driving logic circuits D. The voltage gain of the post-amplifier is approximately g_{m2}/g_{m3} and the gain-bandwidth (GBW) product is

$$GBW = \frac{g_{m2}}{C_{G4}} \qquad (1)$$

where the gate capacitance C_{G4} of the limiting stage is assumed to dominate the load. If inverter Mn4/Mp4 is the same size as Mn2/Mp2, then the GBW is comparable to the unity gain frequency of the NMOS/PMOS combination, which we have treated as a single equivalent transistor.

We suggest an alternative approach, which retains the front-end of Fig. 1A, but uses a post-amplifier based on a transconductance-transimpedance cascade. A particular implementation of this approach, suitable for use in an optoelectronic VLSI context, is shown in Fig. 2. The transconductance stage Mn2a/Mp2a is matched to the front-end, and, as before, the receiver is DC coupled to keep the layout area small. A well-resistor is used as a feedback element in the transimpedance stage Mn3a/Mp3a, in preference to a MOSFET in the ohmic region, to provide reasonable linearity for large output voltage swings and compatibility with a digital CMOS process.

At the internal node X of this amplifier, the signal is represented as a current driven into the low-impedance input of the transimpedance stage. Provided the circuit does indeed operate in the current-mode at this node, the overall voltage gain of the cascade is $g_{m2}\ R_F$ and it can be shown that, for large gains, the GBW in the dominant pole approximation is about:

$$GBW = \frac{g_{m2}}{C_F + (C_{G3} + C_{G4})/A} \qquad (2)$$

where A is the voltage gain of (identically sized) inverters 2 and 3 and C_F is the parasitic feedback capacitance of the transimpedance stage. Thus, in common with other current-mode circuits [6], this configuration can exceed the GBW limit of a single voltage gain stage, and, in particular, has the potential to offer a higher gain than the circuit of Fig. 1 at a similar bandwidth. Of course, a post-amplifier comprising several voltage-gain stages can also exceed the GBW attainable from a single stage.

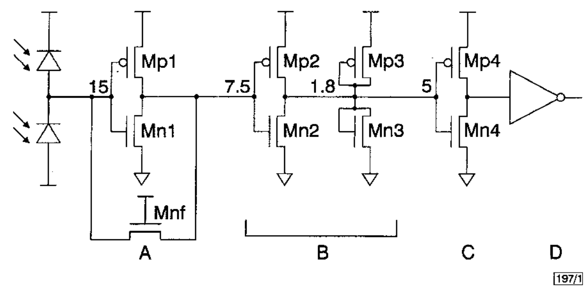

Fig. 1 *Wideband photoreceiver circuit with conventional second-stage amplifier*

Transistor widths are indicated in micrometres
A Transimpedance front-end (Mn1/Mp1)
B Single-stage low-gain voltage post-amplifier (Mn2/Mp2, Mn3/Mp3)
C Limiting inverter with digital output (Mn4/Mp4)
D Digital logic circuitry

Simulation: To compare these techniques in this application, receiver circuits have been designed in a 0.6μm digital CMOS process using a 5V supply. We considered both one- and two-stage versions of the low-gain voltage amplifier approach. The two-stage version (not shown) used an additional inverter with a diode-connected load in stage B of Fig. 1.

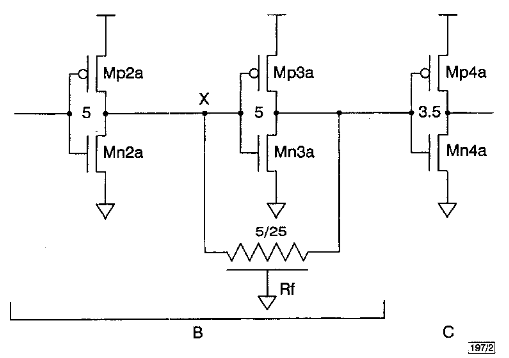

Fig. 2 *Transconductance-transimpedance post-amplifier B with load C, replacing B and C in Fig. 1*

The circuits were specified to operate with a photodiode capacitance of 53fF per diode [7] at 1Gbit/s; we expected the high bit rate to favour the transconductance-transimpedance design. A simple front-end, common to each circuit, was employed. The limiting inverters C were loaded with identical three-stage digital buffers driving an MQW modulator pair to form a simple optical repeater as in [5]. The post-amplifiers were then independently optimised for sensitivity.

Small signal modelling of the post-amplifiers was not appropriate because of the large signal swings and pattern dependent effects at the output of the limiting inverter. Consequently, sensitivity was defined in terms of the peak input photocurrent per photodiode I_{PEAK} required to produce a 500ps eye opening in the transient waveform at the modulator drive output with a $2^9 - 1$ bit pseudo-random input sequence. All circuits would suffer an additional sensitivity penalty due to random noise, estimated to be typically 0.5μA. However, the design constraints imposed by the application meant that the receiver circuits did not attain the noise-limited performance of a standalone telecommunications receiver. In particular, the random DC offset between the front-end and the second-stage amplifier limited the performance.

Simulations were performed using HSPICE BSIM 3v2 models over a range of MOSFET and well-resistor process corners. The effects of offset voltages of ± 25mV (representative of the extremes which might be encountered in a large array of receivers) were investigated. Routing capacitance was neglected.

Table 1: Sensitivity of optimised circuits (excluding noise penalty)

	Sensitivity I_{PEAK}				Power dissipation
	Worst-case process		Typical process		
	0mV offset	±25mW offset	0mV offset	±25mW offset	
	μA	μA	μA	μA	mW
Voltage gain (single-stage)	11.0	21.5	6.7	12.0	9.8
Voltage gain (two-stage)	5.9	15.0	2.2	9.2	12.3
Transconductance-transimpedance	5.9	11.1	2.5	7.2	9.7

Results: The performance of the optimised designs is summarised in Table 1. The power consumption includes the front-end (5.5mW) but excludes the digital driver chain D. The power consumption of all the circuits is sufficiently low to make several hundred element arrays practical, although we did not consider power consumption in the optimisation.

Selected transistor widths of the optimised designs are indicated in the Figures. The front-end widths were chosen to be a multiple of the second-stage widths to reduce overshoot in the front-end response. We also found that a slightly higher GBW could be obtained from the voltage-gain designs by sizing the gain devices Mn2/Mp2 larger than the input devices Mn4/Mp4 of the following stage.

The optimised transconductance-transimpedance postamplifier had an overall voltage gain of ~11. The nominal feedback resistance was 18kΩ. In contrast, the optimised voltage gain amplifiers were forced to use a much lower gain per stage (approximately ×3.3) to support the bit rate.

Discussion: The transconductance-transimpedance design demonstrated almost a factor of two improvement in sensitivity over the most sensitive single stage voltage-gain design. It was also slightly more sensitive than the two-stage design when assessed according to the optimisation criterion (sensitivity on the worst-case process corner with offset). However, the power consumption of the two-stage design was somewhat higher. Two-stage designs of comparable power consumption that were assessed were less sensitive. Another disadvantage of the two-stage voltage amplifier is that the offset voltage between the two stages would make a significant contribution to the input-referred offset because of the low voltage-gain of the first stage. This is not true of the transconductance-transimpedance design because of the current representation of the signal at the internal node.

An important disadvantage of the transconductance-transimpedance design in this application is the layout area required by the well-resistor. The receiver occupied 47 × 29μm² against 25 × 29μm² for the single-stage voltage-gain design. This is still compatible with the requirements of large receiver arrays, but would not be suitable for low bit rate applications where the more compact, single-stage voltage gain design can provide acceptable gain and still support the signal bandwidth. However, this study indicates that the transconductance-transimpedance design is worth considering in systems that require high bit rate channels.

We have found a modified form of the presented circuit to be useful in the design of an experimental crossbar switch in CMOS/InGaAs MQW technology [8] (to be reported on shortly).

Conclusion: We have investigated the suitability of a transconductance-transimpedance post-amplifier in wideband DC-coupled optoelectronic VLSI receiver circuits. Comparisons by simulation to post-amplifiers based on low-gain voltage amplifiers suggest that the higher gain-bandwidth product of the circuit results in improved sensitivity. We anticipate that the extra layout area required by the circuit will only be justifiable in systems using high bit rates (> 1Gbit/s) on each optical channel.

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Advantages of Al-free GaInP/InGaAs PHEMTs for power applications

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The performance and temperature stability of Al-free GaInAs/GaAs PHEMTs with GaInP as a Schottky barrier is reported. GaInP/GaInAs/GaAs PHEMTs with a 1μm gate length show an f_{max} value of 76GHz with a maximum drain current of 570mA/mm and a drain-source breakdown voltage of 16V. Moreover, the first results on short gate length devices (0.15μm) yield f_T and f_{max} values of 106 and 203GHz, respectively. In this case, the drain-source breakdown voltage is as high as 8V. These results demonstrate the great potential of GaInP/GaInAs PHEMTs for power applications.

Introduction: Future communication systems require high-power and high efficiency devices. This need has created considerable