Optical components of the smart-pixel optoelectronic connection (SPOEC) project

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Abstract. The optical components of a 64×64 optoelectronic crossbar interconnect are described. The specifications and performance of the bulk, micro-optic, diffractive and thin-film components are discussed.

1. Introduction

The progress of silicon electronics towards faster processors and greater numbers of off-chip connections is projected to lead to a requirement for aggregate data i/o rates in excess of 1 Tbit s^{-1} within ten years [1]. It has been observed that there exist fundamental physical limits on communication rates between chips using conventional metal lines. The bandwidth scales as the aspect ratio of the interconnection (the ratio of the total cross sectional area of a connection to its length). Calculations have shown that the aggregate chip i/o limit may be considerably lower than 1 Tbit s^{-1} for 10 cm long metal interconnects [2, 3]. Free-space optical interconnects offer a solution to this problem and, in addition, can offer the advantages of negligible crosstalk and high interconnect density in 3D. Whilst the possibilities of optical interfacing to silicon chips are recognized, the development of the components and packaging is still progressing. This paper describes an optical system that has been designed to implement very high data rate communication to a silicon chip to demonstrate the possibilities of free-space optoelectronic interconnects.

2. The SPOEC project

The SPOEC project is a European collaborative project which aims at the construction of a 64×64 channel optoelectronic crossbar interconnect to demonstrate optical data i/o to Si-CMOS at aggregate rates in excess of 1 Tbit s^{-1}. A schematic diagram of the system layout is shown in figure 1 below. The operation of the proposed demonstrator is as follows.

The (electrical) input to the system is in the form of 64 parallel channels which drive an array of 8×8 vertical-cavity surface-emitting lasers (VCSELs) at 250 MHz per

channel. The VCSELs are 10 μm diameter devices, operating at 960 nm wavelength. The VCSEL emission is collected by a two-stage collimation process, described more fully below, and routed through an 8×8 fan-out element to the InGaAs/CMOS switching chip shown on the right of figure 1. The optoelectronic switching chip is constructed from an InGaAs-based strain balanced multiple quantum-well structure, fabricated into detectors and modulators. This chip will be solder-bump flip-chip bonded to a custom designed Si-CMOS chip. The detectors and modulators on the optoelectronic chip are arranged as an 8×8 array of superpixels, each superpixel being composed of an 8×8 array of detectors on a 150 μm pitch with a pair of differential output modulators located in the superpixel centre.

Each superpixel receives a replica of the 64 input channels and the data are routed to the appropriate output modulators by the silicon circuitry. The silicon chip is responsible for header recognition, and data-transparent packet switching. Clock signals are also distributed to each superpixel optically. The aggregate optical data rate to and from the silicon chip has as its target $64 \times 64 \times 250$ Mbit s$^{-1} = 1$ Tbit s^{-1}. The output modulators are read by a Nd:YLF laser beam and the output data streams are routed by polarization to an output chip composed of an array of detector pairs (bottom of figure 1).

The individual optical components, their requirements, design and progress to date will now be described.

3. Micro-optics and diffractive optics

Both refractive micro-lenses and diffractive optical elements play crucial roles in the optical design of the SPOEC demonstrator. The emission from the VCSELs contains 95% of the output power in a cone of NA 0.17. To collect this with
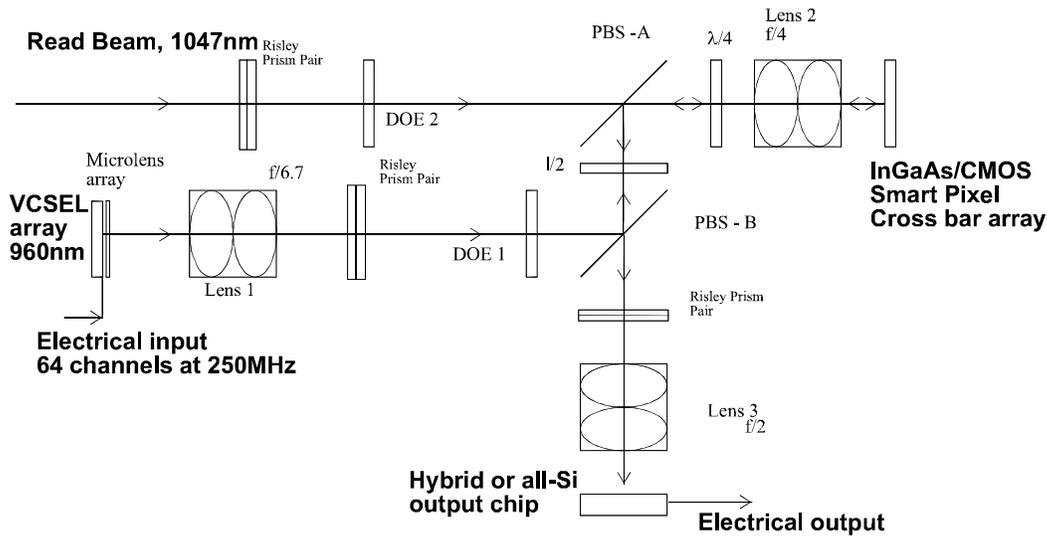
Figure 1. Schematic representation of the SPOEC demonstrator system.

a single bulk lens would present challenges to later optical elements so it was decided to split the collimation function between an 8 × 8 array of f/5.5 refractive micro-lenses of diameter 162 μm and the following bulk lens. The fused-silica micro-lenses are operated at f/3 to reduce the NA of the beams to 0.075, facilitating the later demagnification (see below).

Diffractive optical elements are used to replicate the 64 input signals and to provide read-beam array generation [4]. On the input arm of the system, between the VCSELs and the switching chip, a 1–8 × 8 fan-out is performed by a binary phase-only grating. Binary gratings will be used despite their lower efficiency compared to multi-level gratings, because they allow very efficient zero-order suppression which is needed to avoid crosstalk. On the output arm, the beams used to read the output modulators on the switching chip are produced by an 8 × 16 array generator in the form of a binary phase grating optimized for 1047 nm. One consequence of the use of diffractive optics in an optoelectronic interconnect is that wavelength stability (and uniformity over an array of VCSEL sources) is critical to ensure correct alignment onto detectors. We estimate the uniformity requirement across the VCSEL array to be $\Delta\lambda < 1$ nm.

4. Bulk optics and optomechanics

The basis of the optical system in the SPOEC demonstrator is the implementation of telecentric 4-f imaging of the input VCSEL array to the InGaAs/CMOS switching chip combined with re-imaging of the switching chip to an output chip. Three multi-element lenses have been specifically designed for this task. These lenses have various specifications, following the numbering in figure 1, as shown in table 1.

Lenses 1 and 2 are five-element telecentric anastigmatic lenses, developed from earlier designs [5] using the CODE V software program†. A schematic of lens-2 is shown in figure 2 above. The output lens, lens-3, is an adaptation

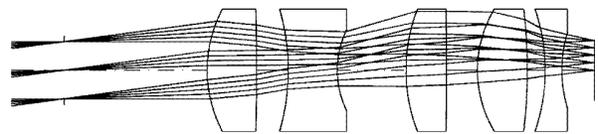† CODE V is an optical design package produced by Optical Research Associates, Pasadena, CA, USA.

Figure 2. Ray-traced schematic of lens-2 showing the telecentric stop and image planes.

of a design by Reiley and Sasian [6]. The optical design proceeded from the requirement for lens-2 to be well-corrected over a large field (15 mm diagonal). This requirement, together with the spot size limitation imposed by detectors of less than 30 μm diameter, led us to choose to design an f/4 lens after working through the trade-offs inherent in lens design [7]. Having specified an f/4 lens-2, lens-1 was then required to be f/7 to demagnify the data channel separation from the 250 μm VCSEL pitch to the 150 μm detector pitch on the switching chip. This f/number requirement for lens-1 necessitates the use of micro-lenses on the VCSEL chip since the f/7 lens-1 on its own would collect only ~40% of the VCSEL emission. In turn, a further demagnification is desirable between the switching chip and the output chip to minimize the area of the output chip.

A particularly demanding aspect of the bulk lens design is the necessity of achromatizing lens-2 over the wavelength range 960–1047 nm to ensure an identical focal length for both the input (VCSEL) and read (Nd:YLF) beams. To date this has been achieved to better than one part in 2000 but further improvement is expected before the lenses are manufactured.

The optical components will be mounted using proven slot-plate technology [8]. A baseplate has been designed with V-grooves in which the barrel mounted components will sit. The advantages of this scheme include the ease of focal adjustment combined with good stability. The three circuit boards holding the VCSEL, switching and output chips will be mounted on adjustable brackets for fine angular and positional control. The entire optomechanical system will fit into a box approximately 30 cm × 20 cm × 10 cm in dimension.

Table 1.

	F/#	Focal length (mm)	Field (mm)	Optimized at wavelength(s) (nm)
Lens 1	6.7	100.5	3	960
Lens 2	4.0	60.0	15	960 and 1047
Lens 3	2.0	30.0	8	1047
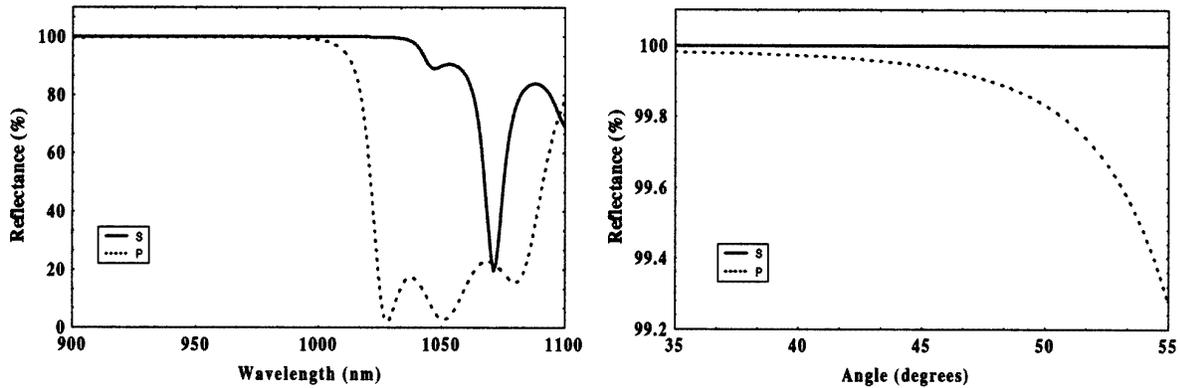
Figure 3. Design performance of thin-film PBSs in both wavelength (at 45°) and angle around 45° (at 960 nm wavelength).

5. Beam splitters

The beam-steering in the SPOEC demonstrator is required to discriminate between the two wavelengths used, 960 nm and 1047 nm. The 1047 nm beam from the Nd:YLF read laser is polarized and can therefore be steered using conventional techniques of polarization rotation combined with the use of polarizing beamsplitters (PBSs). The InGaAs VCSEL array, however, is not polarization controlled [9]. This requirement for the two beamsplitters (labelled PBSA and PBSB in figure 1 above) is that they act as PBSs at 1047 nm and as polarization independent reflectors at 960 nm to route the VCSEL emission efficiently. In addition, the large number of beams incident on the switching chip, combined with the degree of fan-out, leads to a requirement that these beam-splitters operate over the relatively wide incident range of ±7.5°. The design criteria incorporated the need for efficient routing of the 960 nm VCSEL emission, which can be traded off against less efficient polarization routing of the 1047 nm read beam.

The approach that has been taken is to use a thin film coating [10] on a 45°-angled substrate, rather than cubes. The coating contains approximately 30 layers and is approximately 5 μm thick. The design performance is presented in figure 3 and shows that we expect to achieve the required attributes listed in the previous paragraph. Evaluation is in progress on test films and the results correlate well with the design shown here.

6. Summary

The design of the optical components of the SPOEC demonstrator has been presented. The manufacture of the various components is ongoing and we will report both component and initial system test results soon.

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