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Optoelectronics-VLSI system integration Technological challenges

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Abstract

Hybrid VLSI-optoelectronics, also called smart-pixel technology, exploits the respective strengths of optics and electronic processing for the production of optical information processing systems of high performance. The recent integration of micron-size optoelectronic components such as emitters, photodetectors and spatial light modulators within VLSI electronic chips allows the fabrication of on/off chip data communication rate systems of the order of 10^{12} pin-Hz. This aggregate rate is at least one order of magnitude higher than is presently achievable in electronics alone. Several issues, however, remain to be resolved in order to fully benefit from this technology. These include the relevance of optics in information processing in general and computer science in particular, the design and choice of the logic complexity of the electronic circuitry, its interfacing with optoelectronic components, the assembly and testing of the resulting systems. These technological challenges are discussed in this article in the light of the rapid progress achieved in this field.

Keywords: Smart-pixel technology; Optical interconnects; Hybrid-VLSI optoelectronics; Optical information processing; Optical computing; Optoelectronics

1. Introduction

Over the last 15 years, the optoelectronic community has witnessed a constant drive towards the full integration of optoelectronic components within their associated VLSI electronic processing circuitry. This trend, originally fuelled by the long-haul telecommunications industry, (A) in Fig. 1, was geared towards the fabrication of OEICs (Opto-Electronic Intergrated Circuits) [1]. More recently, the need for more aggregate data bandwidth in optical information processing systems has initiated numerous industrial and academic research in the design and fabrication of interboard, inter- and intra-chip interconnection schemes. The resulting devices ((C) and (D), Fig. 1), called smart pixels or optoelectronics-VLSI components, benefit from the strengths of optics in data transmission (huge I/O photonic density, immunity to electromagnetic interference, large fan-out capability, automatic impedance matching, power savings at long distance, real-time reconfigurability) and the processing power of VLSI electronic circuits [2,3]. Today, demonstrators based on this technology exhibit the same aggregate bandwidth as that foreseen with electronic systems for the year 2007 [4]. This remarkable achievement is rendered possible by a variety of factors: (1) the integration of micron-size optoelectronic transceivers with VLSI circuits; (2) the massive parallelism offered by free-space optics; (3) a better understanding of the added-value of optics in information processing systems; and (4) the progress in low-cost optical assembly, testing and packaging. In all these domains, however, technological issues mar the full potential of this technology: (1) the interface of optoelectronics with silicon-based VLSI circuits is still technologically immature; (2) the alignment and fabrication limitations faced by free-space optical components could be bettered by the adoption of existing solutions and established standards; (3) the slow progress in adopting optics in computer architecture is symptomatic of the general lack of knowledge of optics by computer scientists as well as the ignorance of computer science by optical engineers; (4) the difficulty in assembling and testing fully functional prototypes is due to the requirement of feeding a vast amount of vector tests; and (5) the inter-disciplinary nature of

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overall systems require large teams of experts with different educational backgrounds.

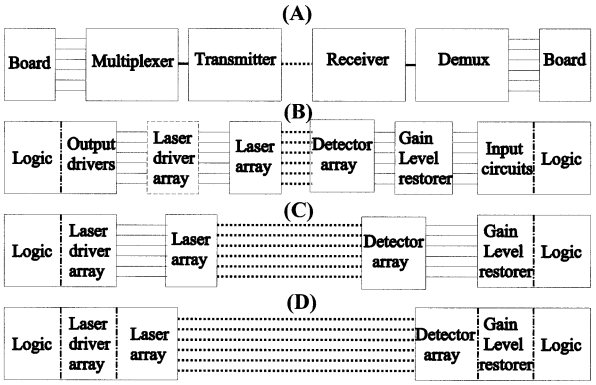

Fig. 1. Historical perspective in optical interconnections in optical information processing systems (solid lines: electronic connections, broken lines: optical connections). (A) and (B) was originally encountered in long-haul telecommunications systems. (C) and (D) is generations of VLSI-optoelectronic systems, which are being actively researched (after [1]).

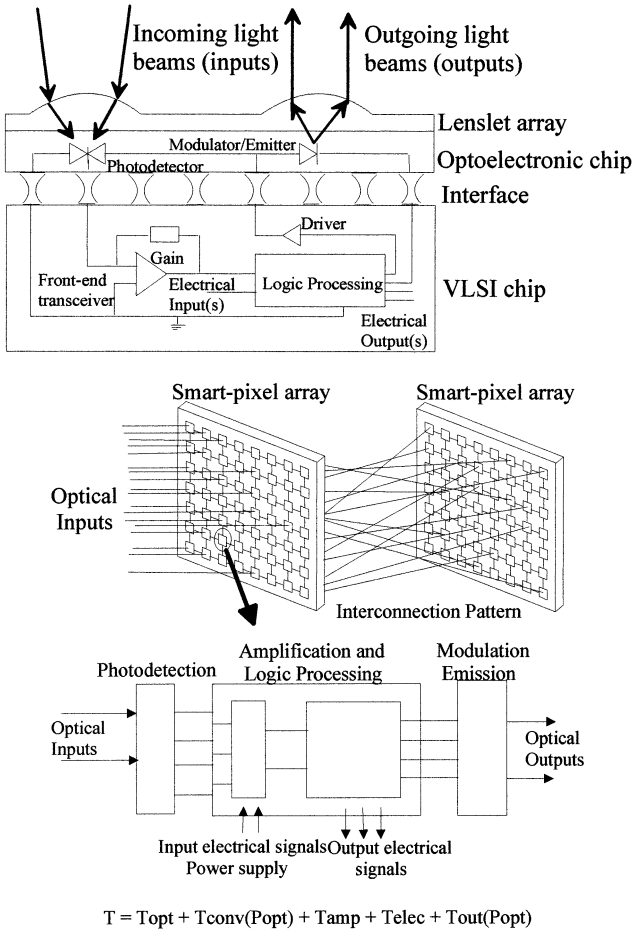

Fig. 2. Physical and functional schematics of a generic optoelectronic-VLSI component.

2. Optoelectronic-VLSI components: generalities

All smart-pixel devices, irrespective of their underlying electronic logic family and optoelectronic interface, receive, modulate or emit information in the optical domain and process it in the electronic domain. Physical and functional schematics of a generic smart-pixel are given in Fig. 2.

Optical data streams are input into one or several photodetectors, which convert the beam intensity into photocurrent. Most optical schemes rely on binary intensity modulation. The converted current signals are then amplified (either by a current or a voltage amplifier) and processed electronically. The resulting output data drive modulators (voltage variation) or emissive devices (current variation). Most of the exampled modulators, nowadays, are based on multiple quantum well structures and exploit the quantum-confined stark effect [5]. Photodetectors include the same class of modulators used as PIN photodiodes, metal–semiconductor–metal (MSM) detectors or photoconductive devices. The emissive devices can either be light emitting diodes (LEDS) [6] or, more frequently, vertical cavity surface emitting lasers (VCSELs) [7,8]. Emitters, modulators and photodetectors can be fabricated on the same substrate, which is usually different from the silicon substrate devoted to electronic processing. As a result some interfacing technique is needed to connect the optoelectronic inputs to their electronic counterparts. In the pursue of full integration, a further lenslet or hologram array can be fabricated or interfaced on top of the electronic chip in order to collimate or steer the ingoing and outgoing optical beams.

The amplification stage is usually not noise-limited and ranges from the simple but capacitance-limited voltage gain amplifier [9], the transimpedance amplifier [10] and some variations from it [11] to the sophisticated charge- or current-sensed amplifier [12]. Arrays of perhaps up to 10^4 (usually) identical pixels, occupying roughly the same chip area as the underlying electronic chip, are interconnected to other chips using free-space or guided wave optics whereas logic and local on-chip interconnection is electrical. The logical processing stage is usually devoid of R^3 (recovery, retiming, reshaping) electronic circuitry because of the limited amount of silicon real estate at each pixel. The number of electronic gates per pixel dictates the smartness, i.e. the logic complexity of the demonstrator. The electronic logic family can range from GaAs-based direct coupled FET-logic to standard Si-CMOS as shown in Table 1. The tasks performed by some of the demonstrators' range from primitive image operations such as noise removal to more complex functions such as systolic processing [13] as shown in Table 2.

Table 1
Example of technologies used worldwide in optoelectronics-VLSI systems

Group and demonstrator system	Input array	Electronic logic family	Output array
Lucent Technologies (switching chips)	GaAs PIN diodes	Si-CMOS	GaAs MQW modulators
Heriot–Watt University (bitonic sorter/crossbar)	InGaAs PIN diodes	Si-CMOS	InGaAs modulators, GaAs VCSELs
MIT (optical neural network)	MSM-GaAs	Direct Coupled FET Logic	Epitaxy on Electronics GaAs/InGaP LED
McGill University (optical backplane)	GaAs PIN diodes	Si-CMOS	GaAs MQW modulators
Georgia Tech (ADC converter)	MSM-GaAs	Si-CMOS	Not applicable
UC Boulder (board to board pipeline)	MSM GaAs	Si-CMOS	GaAs VCSEL
University of Edinburgh (intelligent display)	Not applicable	Si-CMOS	Liquid crystal display on silicon
UC San Diego (optical transpose interconnect system)	MSM GaAs	Si-CMOS	GaAs VCSEL

Table 2
A classification of some smart-pixel demonstrators in terms of logic complexity and functionality

Logic complexity	Functionality	Research group
Photodetection	Thermal imaging	Commercial use
Primitive operations	Artificial retina	Institut d'Optique Applique (France)
Routing	Optical crossbar/sorter switch matrix	Heriot–Watt (Scotland), Lucent Technologies (USA), McGill University (Canada)
SIMD processor	Systolic processor	Georgia Tech (USA)
ADC	Image processor	Georgia Tech (USA) United States Military Academy (USA)

Optoelectronic-VLSI benefit from several advantages:

1. The design and construction of high-aggregate bandwidth systems is enabled through the massive parallelism of the dense space-multiplexed array of optoelectronic components [14].
2. A lower cost of interconnect is thereby permitted by the optical addressing of the transceivers in the third dimension. The move to higher pin-count is therefore facilitated.
3. The partitioning into separate domains (electrical and optical) of signal and power supply (and ground) I/Os eases the reduction of electronic crosstalk and switching noise.
4. Data-acquisition and data addressing to other hardware (such as optical memories) can be parallel.
5. The power consumption of off-chip interconnections is lower than for terminated wires due to the inherent impedance matching of optical terminations [15]. For example 30% savings of on-chip power dissipation, compared to an all-electronic version, has been demonstrated by the use of an optical distribution scheme [16].
6. The global optical distribution of a clock allows the formation of isochronous regions inside a wire-limited VLSI chip [17]. This property could allow the design of low access time DRAMS [18].
7. The reconfiguration of non-local, space-variant interconnect patterns become feasible on a single-cycle timescale, allowing thereby greater freedom in the design of more efficient computer architectures and algorithms.
8. Significant savings in shielding cost of the electronic equipment are rendered possible since the optical transmission of information does not undermine the signal integrity.

3. Logic complexity and design issue

Optoelectronics-VLSI technology is inherently a multi-disciplinary field. The building of systems require the gathering of experts such as optical hardware designers, opto-mechanics engineers, semiconductor (optoelectronic) manufacturers, system architects, computer scientists, VLSI circuit designers in the digital and analogue domains, specialists in hybrid integration, assembly engineers, packaging and testing engineers. Research groups tend consequently to be very large and to have sufficient resources for the fabrication of prototypes. The diversity of backgrounds, albeit intellectually enriching, can however be an impediment in the design process as few people can claim a thorough mastering and understanding of the overall design and fabrication process. Recently in Europe, a series of workshops

sponsored by the European Commission were organised to attempt to throw bridges between the optical engineers and computer scientists. The results of these discussions show how subtle and unexpected the benefits of optics can be in specific monoprocessor and multiprocessor architectures [19]. The list shown in Table 1, which is by no means exhaustive, shows the diversity of technologies tried on and is a reflection of the immaturity of field as well as the wealth of possibilities. In recent years, however, Si-CMOS seems to be the preferred logic electronic family due to the achievable gate density and the rapid progress of electronics. On the optoelectronic side, III–V semiconductors based modulators and VCSELs are used due the maturity of the device fabrication process for the former and the device advantages for the latter.

In microelectronics, chip design involves a series of trade-offs between die area, chip functionality and performance, speed and power use. In optoelectronics-VLSI, the available optical power, P, at the photodetectors need to be accounted for. This optical power dependence will determine the minimum processing time, T, available, that is the maximum pixel operating frequency (Fig. 1). One of the major challenges is the tackling of these constraints in order to determine the optimum pixel smartness, that its logic complexity, such as to maximise the overall system performance. For example, complex pixels with large number of electronic gates require large silicon, very few of such pixels can be accommodated on a single die. The resulting low parallelism introduced by this low granularity may not take benefit from the data transmission by optics. In the other extreme, too many pixels of primitive functionality may require costly optical and optomechanics hardware in order to implement the optical addressing. It is in fact possible to show that the optimum performance of hybrid processing elements depends on a narrow set of parameters that is independent of the architecture and technologies used [2,3]. This set of parameters, shown in Table 3 with some case studies, dictate that the optimum system performance occurs when the optical data-rate per data channel matches the electronic processing rate. The smart-pixel array would not make use of the optical bandwidth offered by optics if it has a low number of optical channels, unless multiplexers and demultiplexers are employed. A higher number of channels would reduce the optical energy available per channel in modulator-based systems, which would force the electronic receiver to operate at a lower operating frequency then predicted. The data used in Table 3 can accommodate the changes of technology. For example, if only 1 pJ switching energy detectors were only available, the optical data-rates available would be one order of magnitude lower than the shown case. The 10^4 channels could only be operated at 100 GHz communication rate and at 10^{13} gate-Hz. As indicated by the table, the niche lies in the region of 100–1000 gates per channel and 10^3–10^4 pixels per chip. As crude as the model can be, the characteristics of current demonstrator systems have pixel number ranging from 1024 to 4352 [9,20], each of which encompasses between 36 and 300 gates. The bitonic sorter built at Heriot–Watt University display a maximum communication rate of about 5.10^{11} pin-Hz, which is close to the number calculated above [9].

Table 3
Bird's-eye view of smart-pixel technology

Electronic domain				
Electronics switching energy, E_e (pJ)	0.1			
Maximum heat dissipation Q (Wcm^{-2})	100			
Electronics frequency, F_e (MHz)	100			
Number of gates per cm^{-2}	10^6			
Gate-switches per chip (gates-Hz)	10^{14}			
Optical domain				
Optical conversion energy, E_o (pJ)	0.1			
Source average power, P_o (W)	1			
Source-to-detector efficiency, η	0.1			
Communication rate (pin-Hz)	10^{12}			
Number of (optical) input pins	10^2	10^3	10^4	10^5
Potential optical data rate per pin (MHz)	10^4	10^3	100	10
Potential electronic frequency (MHz)	100	100	100	100
Number of gates per pin	10^4	10^3	100	10
Gate-switches per chip (gate-Hz)	10^{14}	10^{14}	10^{14}	10^{13}
Communication rate (GHz)	10	100	1000	1000

4. Device integration and interfacing issues

Whereas, in the past, studies on the performance of optoelectronic devices concentrated on the speed and power consumption (Table 4) [8,14,21], recent research attempts to compare their ease of integration within the electronic circuitry [22].

The high bit-rates and low power consumption stem from the technological progress made by the devices themselves and the electronic drivers. The performance of the transceivers actually benefits from the ever-decreasing minimum feature size of VLSI chips. Although the MQW modulator offers the best performance in terms of power dissipated and optical switching energy, the rapid technological progress in VCSELs operating frequency (multi Gbit s^{-1}) and threshold current (sub mA) is likely to render this advantage obsolete.

The difficulty in monolithically integrating emitters onto silicon requires the use of hybrid technology if the electronic processing is not carried out on III–V semiconductor based chip. Table 5 shows an overview of the different techniques used alongside their advantages and their drawbacks.

Table 4
Characteristics of some optoelectronic emitters and modulators [22]

Devices	Optical switching energy/window area (fJ μm^{-2})	Bit-rate (Mbit s^{-1})	Power/Gbit s^{-1} (mW Gbit s^{-1})
S-SEED	200	0.2	N/A
NIPI-modulator	20	1	N/A
Optical Thyristor	0.2	20	N/A
FET-SEED	8	100	120
LED	28	250	20
VCSEL	140	600	23
MQW modulator	3	600	1

Table 5
Advantages and drawbacks of the interfacing techniques

Technique	Advantage(s)	Bottleneck(s)
Wire Bonding	Simple	Low speed, inductance high, low I/O pin count
Flip-chip bonding	Low inductance, surface connection, mature technology	Possible substrate removal and planarisation of optoelectronic chip
Epoxy anisotropic glue	Simple, surface connection	Possible substrate removal and planarisation of optoelectronic chip
Electronic Integration		
Hybrid	No compromise on material	High inductance
Monolithic	Small parasitics	Yield, immature technology
Wafer fusion	Global interfacing	Immature technology
Epitaxial lift-off	No compromise on material	Immature technology

Table 6
Optoelectronic output interfaces characteristics for smart-pixel arrays

Devices	On-chip drive power	Inter-chip connectivity density	Fan-out capability
MQW Modulators	Excellent	Good	Poor
VCSELs	Fair	Moderate	Excellent
LEDs	Poor	Incompatible with DOEs	Poor
Microcavity LEDs	Good	Use of fibre bundles	Fair

Flip-chip bonding is being adopted by a few research groups wordwide. The small mismatch of the coefficients of thermal expansion between silicon and GaAs does not require, on thermal grounds, the use of underfill. The technology is also mature and is also recently witnessing a revival in the microelectronics industry.

5. System integration issue

As elements of an array, the optoelectronic components have quite disparate optical and electronic qualities as shown in Table 6. The choice of optical transceivers will depend ultimately on the application and the sytem volume. For example the low number of VCSELs that can be put on a chip today (around 64), due to electrical crosstalk and driving capability limits the parallelism of channels although the fan-out performance of such devices is excellent. On the other hand, thousands of modulators can be laid out on 1 cm^2 die, resulting in a high parallelism; the fan-out, however, is poor due to the low output contrast ratio (1.2–3).

Table 7 provides a comparison of the drawbacks of VCSEL-based and modulator-based systems. Two main drawbacks in modulator based systems is the need for an external laser source to read the devices and the necessity to have large voltage swing in order to drive them. On the other hand, VCSEL-based demonstrators have yet to show fully operational arrays of more than 64 devices, all running at several GHz.

6. Assembly and testing issues

The high-aggregate bandwidth of such systems is useful only if the data to be processed can be fed into the system and be output on a timescale comparable with the processing time of the demonstrators. In the case of optical input and/or output data beams, the

problem of connecting such a system to the outside world lies in the concentration of a hundred to a thousand optically parallel, equally spaced channels within a chip-compatible area. This requires precise assembly and optomechanical control of the beams in the case of free-space optics. As an example, Fig. 3 shows the improvement in the collection efficiency of data beams provided by VCSELs, submitted to thermal variations when active alignment is implemented. In this specific case, a liquid prism is used to steer the beams onto specific photodetectors. Active control feedback is provided between the prism and the detectors.

If the data beams are coming or going into optical fibres, dense 2-D fibre array connector would be needed. Such a connector cannot be manufactured at the present in a cost-effective manner. In the case of electrical input or output data streams, the problem lies in the frame-rate limitations of the electrically addressed smart-pixel arrays due to the RC-limitation of the galvanic wires and the limited number of available electrical pin-outs. On-board or on-chip temporary storage in the form of memory registers are needed, for which fully loaded on-chip memory banks are emptied in burst mode into the input array during addressing are refilled, as a background activity, whilst the data are being processed optically. Such situation is also likely to occur for the testing of such systems since present electronic testing equipment are unlikely to cope with the tremendous aggregate bandwidth generated by such systems.

Table 7
Drawbacks of VCSEL-based and modulator-based demonstrator systems

VCSEL-based system	MQW modulator-based system
High current threshold	High voltage swing
Array uniformity (threshold, output power)	Optical bandwidth (narrow wavelength range)
Delay versus bias	'Read' laser expensive (£3–10 per I/O)
Modal characteristics	Optomechanics expensive (£5 K Tb^{-1} s^{-1})
Polarisation control	Temperature stability
Wavelength (850, 980, 1300, 1500 nm)	
Device spacing (thermal, electrical crosstalk)	
Feasibility of co-planar contacts in flip-chip	
Performance degradation after integration	
VCSEL power versus receiver gain	

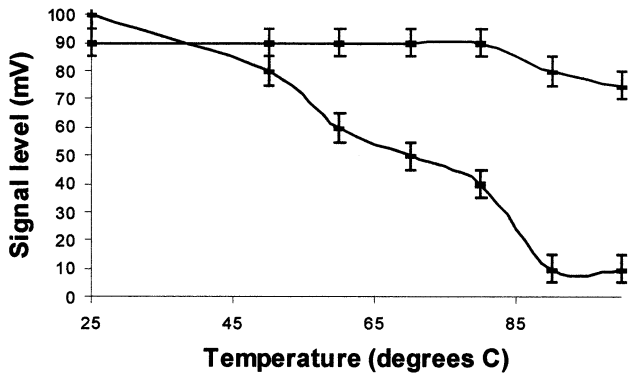

Fig. 3. Active alignment of a VCSEL array by means of a liquid prism. The sloping curve is the signal detected by the photodiodes without correction of the beams. The flat curve is given with the active alignment set up activated.

7. Conclusion

From the seminal work on all-optical computing more than twenty years ago to the current research in optically interconnected electronics, the field of optical information processing has witnessed a shift of interest towards optoelectronic-VLSI systems. Whereas optoelectronic devices have become reliable and show performance factors compatible with electronic processing, more work needs to be carried out on the integration aspects of this technology at the device, interfacing, system, assembly and testing levels. The huge aggregate bandwidth provided by this technology still has to be harnessed and harvested by electrical engineers and computer scientists.

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