An Optoelectronic Crossbar Switch as a Demonstrator Test-Bed for Terabit/s i/o

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Introduction and System Architecture

It is predicted that the i/o requirements of future generations of integrated circuits will exceed one terabit/s [1]. Calculations indicate that electrical connections will be fundamentally limited at such bandwidths over distances in the range of several centimetres [2]. Optoelectronic-VLSI (OE-VLSI) - the integration of surface-normal optoelectronic devices with VLSI electronics using hybridisation methods such as flip-chip bonding - potentially offers a solution. We describe the completed design of a demonstrator system being developed to investigate the free-space optoelectronic interconnection of silicon VLSI chips with aggregate i/o data rates in the Tbit/s domain [3].

The system architecture is a packet-switched optoelectronic matrix-matrix crossbar [4]. Sixty-four electrical signals are converted into optical signals by an electrically addressed 8-by-8 VCSEL array. Each of the 64 optical outputs from the array are themselves fanned out 64 times by an 8-by-8 fan-out diffractive optical element (DOE). The resulting set of 4096 optical signals is relayed to a hybrid InGaAs/Si OE-VLSI chip which is partitioned into 64 blocks or "super-pixels". Each super-pixel receives the full set of 64 optical input signals and converts these into electrical signals which are electrically routed by the silicon-based 0.6 μm CMOS circuits that are flip-chip bonded to the InGaAs-based optical interface chip. The unique output from each super-pixel, which represents the one signal selected from the original set of 64, is converted back into an optical output by means of a differential pair of multiple-quantum-well modulators. So as to complete an output electronic interface, the 64 output optical signals are relayed to another hybrid chip composed of an array of photoreceivers flip-chip bonded onto a second silicon integrated circuit. The system is designed as a packet switch with the routing chip configured by the packet header. Arbitration is handled internally by means of a cyclic priority scheme. Two of the inputs are used for the (differential) clock signals which are distributed optically to each super-pixel.

System Input by Vertical Cavity Surface Emitting Laser (VCSEL) array

The electrical inputs to the demonstrator are converted to optical signals by an 8x8 array of top-emitting MOVPE-grown VCSELs. These consist of 30.5 pairs of λ/4 thick $Al_{0.9}Ga_{0.1}As$ and GaAs layers for the bottom Bragg mirror and 22 pairs for the top mirror. The cavity is 270 nm long including three 8 nm wide $In_{0.13}Ga_{0.87}As$ quantum wells separated by 10 nm wide GaAs barriers. A λ/2 thick GaAs contact layer concludes the structure. The 10 μm diameter VCSELs are on a pitch of 250 μm. The measured capacitances of the centre VCSEL (longest wiring) and border VCSEL (shortest wiring) are 3.05 pF and 1.05 pF, respectively.

The DC electrical and optical characteristics of the VCSEL array bonded onto their PCB are as follows: mean threshold current 2.6±0.05 mA, mean threshold voltage 1.90±0.01 V and output power (at 8 mA) 1.25±0.02 mW. Fully operational arrays have been fabricated with an emission wavelength

of 956 nm and ±0.7 nm variation at 8 mA current. High frequency operation of the VCSEL array, prebiased at 1.9 V threshold, has been successfully tested with data rates up to 500 MBit/s. Electrical crosstalk has been measured to be below 10%, which was shown to originate from the parallel wiring on the PCB.

The VCSEL array is mounted on a sapphire substrate, on a custom-designed PCB. The VCSEL was modelled as a 105 Ω resistance at the current-voltage operating points (2.6 mA,1.85 V) and (8.0 mA,2.44 V). Using this model, a passive impedance two-port network has been designed to match the 50 Ω driver and the VCSEL load. This gives a compromise between maximum bandwidth and a minimum sensitivity to the variation in the VSCEL characteristics over the array. For 0 and 1 having the same probability of appearing in the data, the heat dissipation is 0.77 W for the VCSEL array and 6.14 W for the PCB. A temperature sensor and Peltier element are included for temperature control.

Optical and Optomechanical Design

The free-space data relay is performed by telecentric *4-f* imaging using custom designed multi-element lenses. The lenses are required to relay the data from the VCSEL input array at 956 nm wavelength to the hybrid OE-VLSI chip detector array via a diffractive fanout element. The principal challenge is to image the VCSELs onto the 35μm diameter detectors over the 17.5 mm diagonal field of the OE-VLSI chip. Readout of the data from the modulator pairs is achieved by means of an external cw Nd:YLF laser at 1047 nm wavelength and these modulator pairs are further imaged onto the output chip as described above. The lens designs have been developed from earlier work [5,6] and are simulated to perform as required with near diffraction-limited performance at each of the two internal wavelengths. The collection of the VCSEL emission is performed by a combination of an integrated microlens array and a bulk lens [7]. A key aspect of the optical design has been the requirement to route the data through the system using a combination of polarisation and wavelength differentiation. The thin-film beam-steering elements fabricated for this task, together with all of the optics and slot-plate optomechanics, are further described elsewhere [8].

InGaAs-based Modulator and Detector Arrays

The III-V semiconductor optoelectronic interface arrays consist of differential modulator pairs and single-ended detectors. The two diodes in the differential output pair use a common n-type bias voltage and separate digital driver circuits are used to drive the two p-type contacts with the true and complementary data. Compared to the conventional approach of two series-connected modulator diodes, this approach reduces switching noise on the modulator bias voltage, but requires larger silicon driver circuits to sink the total photocurrent through each diode of the pair rather than the difference between the two. The modulator bias voltage is separated from the detector bias to avoid electrical crosstalk and to permit separate optimisation.

The arrays are fabricated from In(Al,Ga)As strain-balanced multiple quantum well (MQW) p-i-n structures grown by molecular beam epitaxy (MBE). The structures are deposited on GaAs substrates with an intervening buffer layer 2μm thick containing a linear grade in In concentration. The top p^+-InGaAs contact layer includes Be δ-doping to facilitate the formation of low resistance, non-alloyed ohmic contacts. Fuller details of the MBE grown MQW layers have been described in [9]. The processing of the arrays includes (1) mesa isolation of the individual devices by a two-step wet chemical etch; (2) lift-off of a sputtered gold film with a bi-layer photoresist to form non-alloyed contacts to the detectors and modulators (the gold film serves the additional purpose of a high reflectivity mirror); (3) trench isolation of the lower n^+ contact layer to disconnect electrically the modulators and detectors, and (4) overall passivation with PECVD SiO_2. Test diodes indicate turn-on voltages ~ 0.8 V and reverse saturation currents of <10 nA for a mesa with a diameter of ~35 μm. The modulators used in the demonstrator system are designed to operate with the available 5 V. There is a clear trend to decreasing voltages being used in the underlying silicon CMOS. Thus modulator design at lower voltages is an important issue, as is improved modulator performance at the present 5 V bias. The incorporation of an optical cavity in the design is being pursued to address these questions, with encouraging results [10].

Silicon VLSI design

The silicon component [3] of the OE-VLSI chip has dimensions 14.6 mm x 15.6 mm, and has been fabricated in 0.6 μm technology from Austria Mikro Systems. The chip is packaged on a PGA256 cavity-up carrier. The digital circuit of the OE-VLSI chip operates in two phases: a synchronous address recognition phase followed by an asynchronous routing phase. An asynchronous arbitration circuit is used to configure the 64:1 multiplexer based on the results of the address recognition phase, which determines which of the inputs has an address matching that of the superpixel. Note that using a clock signal only in the decoding phase reduces the power requirement. See [3] for a more complete description of the digital circuit design.

The routing chip uses two types of receivers to amplify the detected photocurrent to standard logic levels. The data receiver is a single ended DC-coupled transimpedance design with an individual power consumption of 2.5 mW and a peak consumption (over the array) of 10 W during the header decoding phase. Prototype circuits show a sensitivity of 5 μA at a data rate of 100 Mbit/s with a sensitivity of 3.5 μA at 200 Mbit/s operation expected from the final design. The clock receiver uses an electrically differential front-end followed by a transconductance-transimpedance post-amplifier [11]. The differential clock circuit allows a simplified InGaAs fabrication process and better immunity to common-mode voltage noise. Crosstalk in the receivers has been addressed by the inclusion of ~2pF of gate-oxide decoupling capacitance in each pixel to filter high-frequency supply noise. The decision stage of the receiver circuit has a separate power supply to isolate it from the front-end post-amplifier. 100 external power supply pads have been used for the analogue supplies to reduce inductance. A detailed study of electrical crosstalk in large arrays has been performed [12].

Summary and Acknowledgements

The system design is intended to demonstrate the technological potential of OE-VLSI in the terabit/s regime without addressing any particular application area. The crossbar architecture conveniently allows high data-rate operation to be tested experimentally with modest numbers of inputs and provides an appropriate test-bed for the technologies that may be applied to the terabit/s scale interconnect challenge.

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