

TERABIT/S OPTOELECTRONIC INTERCONNECTION TO SILICON VLSI

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The very near Future

High Performance ASICs: 1997 US SIA Roadmap

YEAR - first shipped	Feature Size -minimum	V _{dd} (volts)	Number of transistors	Chip Size (mm)	Maximum Dissipated Power	Clock (off- ≈ on- chip)	Total-pins -package Half HF?	Aggregate Bandwidth (off-chip)
1997	250 nm	~2.2	8 M	22 x 22	70 W	300 MHz	1100	165 GHz
1999	180 nm	~1.7	14 M	25 x 32	90 W	500 MHz	1500	375 GHz
2001	150 nm	~1.4	16 M	25 x 34	110 W	600 MHz	1800	540 GHz
2003	130 nm	~1.3	24 M	25 x 36	130 W	700 MHz	2200	770 GHz
2006	100 nm	~1.1	40 M	25 x 40	160 W	900 MHz	3000	1.4 THz
2009	70 nm	~0.8	64 M	25 x 44	170 W	1.2 GHz	4100	2.5 THz
2012	50 nm	~0.6	100 M	25 x 52	175 W	1.5 GHz	5500	4.1 THz

THz i/o
expected by
2005 !

BUT

Bandwidth down wire(s) is limited to B_0

A/L^2 bit/s*

e.g. an MCM has:

$A=0.04\text{cm}^2$, $L=10\text{cm}$

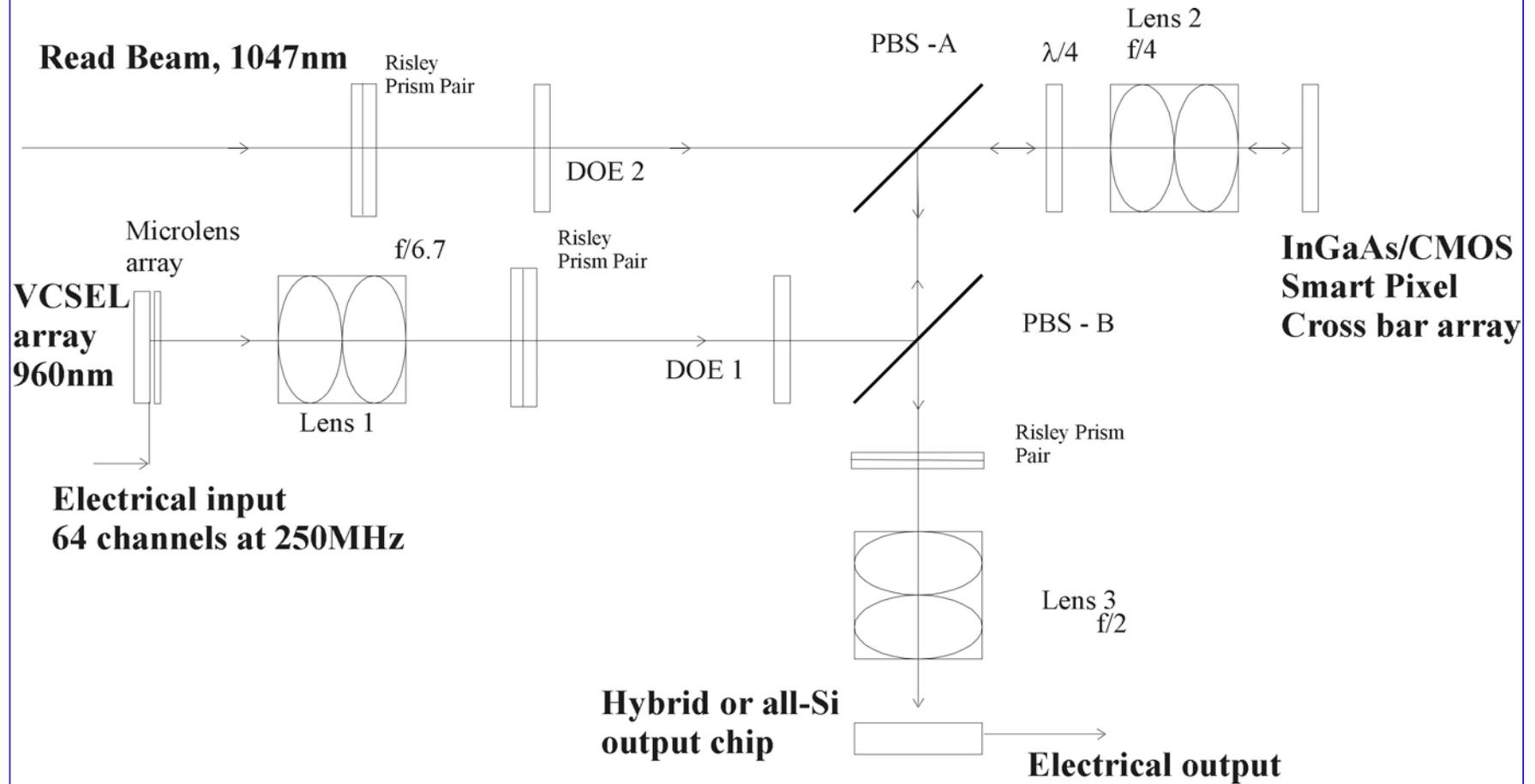
Limit < Tbit/s

Bandwidth

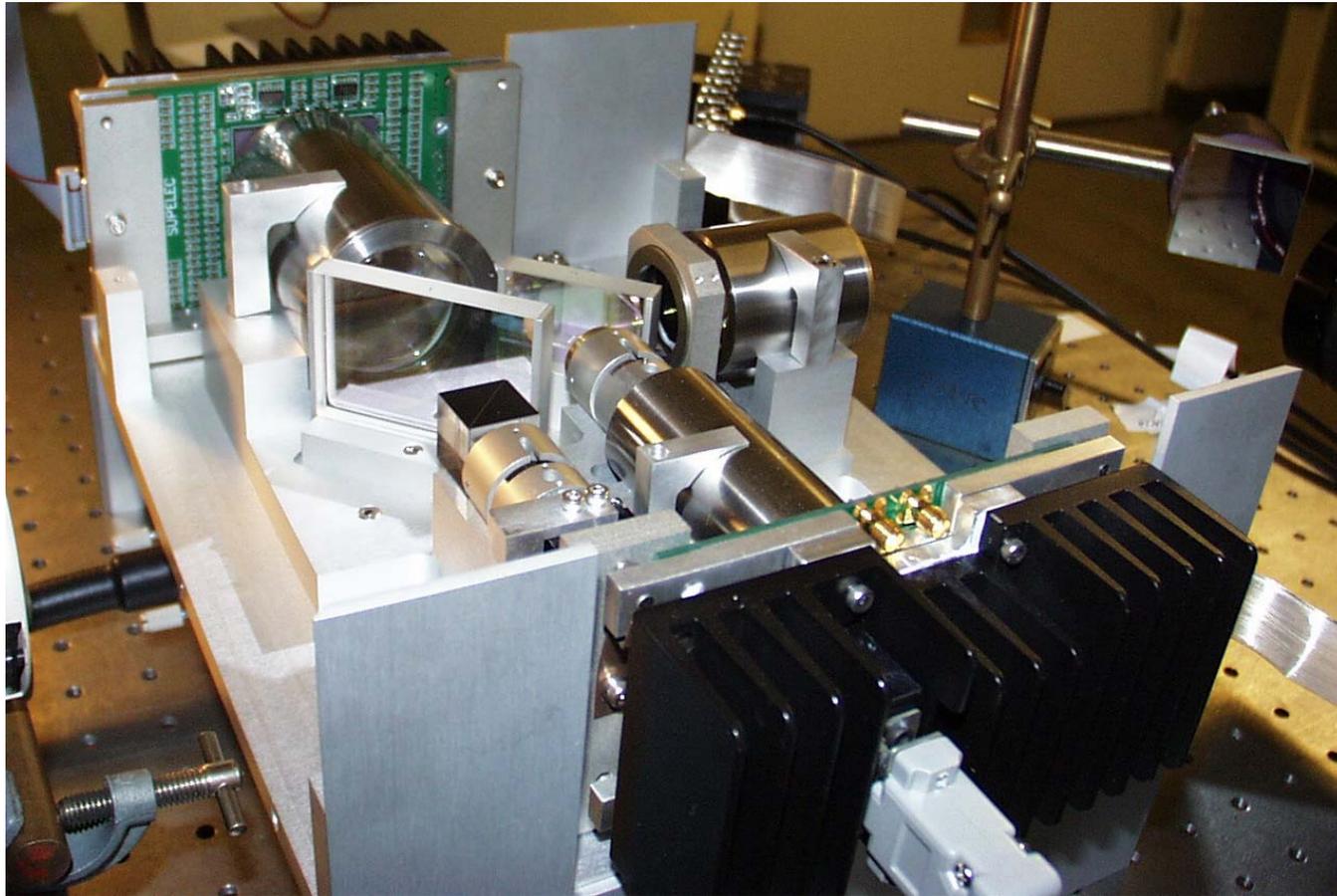
An optoelectronic approach

- ▶ Packet-switched Crossbar Interconnect
- ▶ Free-space Optical Connection to Silicon chip
- ▶ Hardware demonstration of key technologies
- ▶ **Demonstration of Tbit/s i/o to VLSI**

The SPOEC System Layout



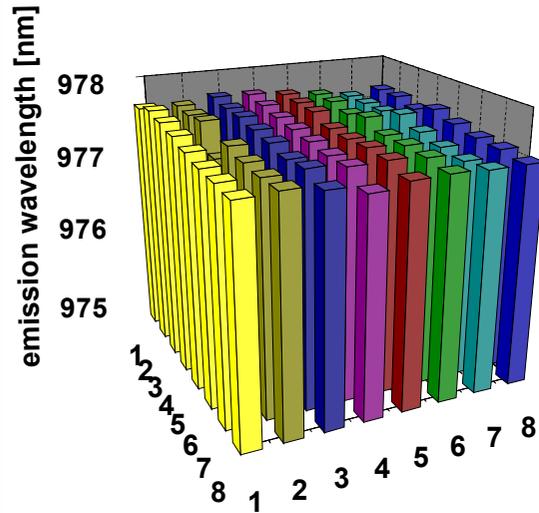
Assembled Demonstrator



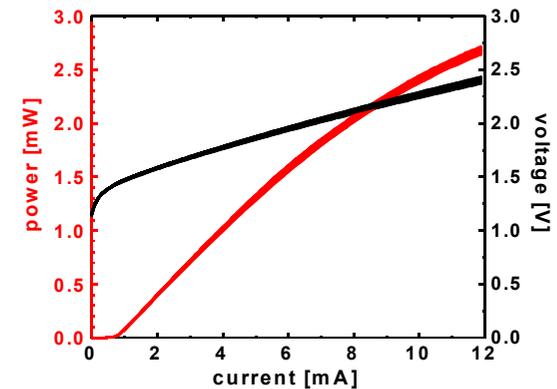
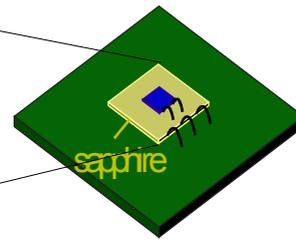
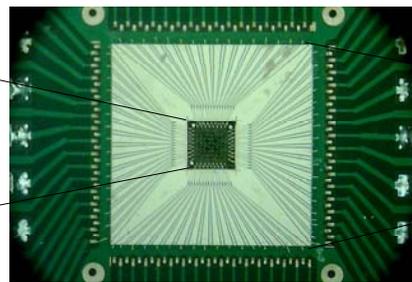
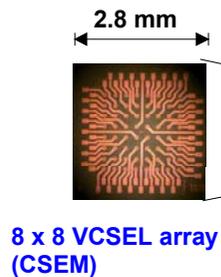
QE-14, Manchester
September 1999



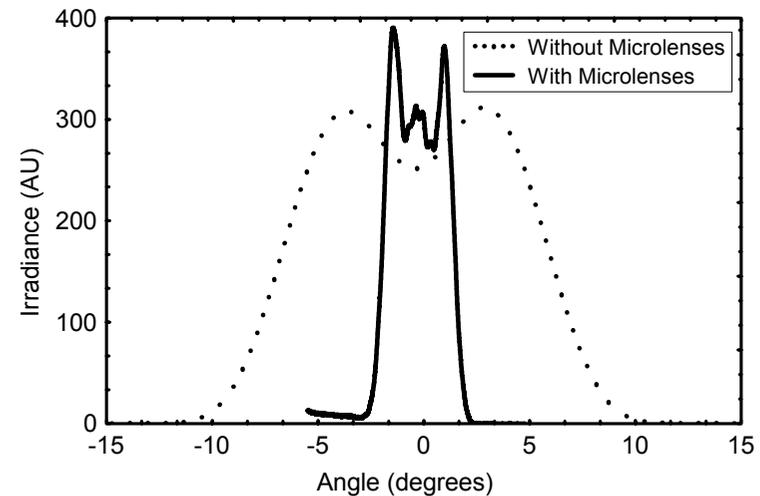
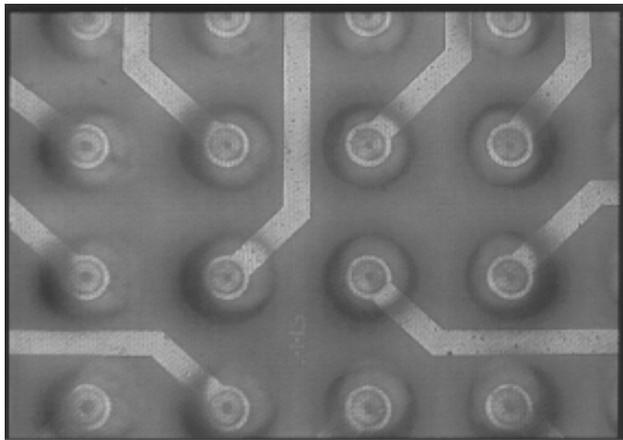
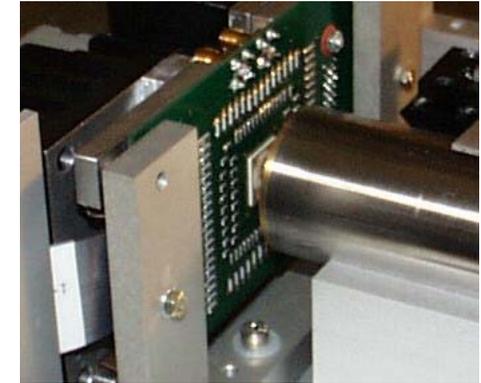
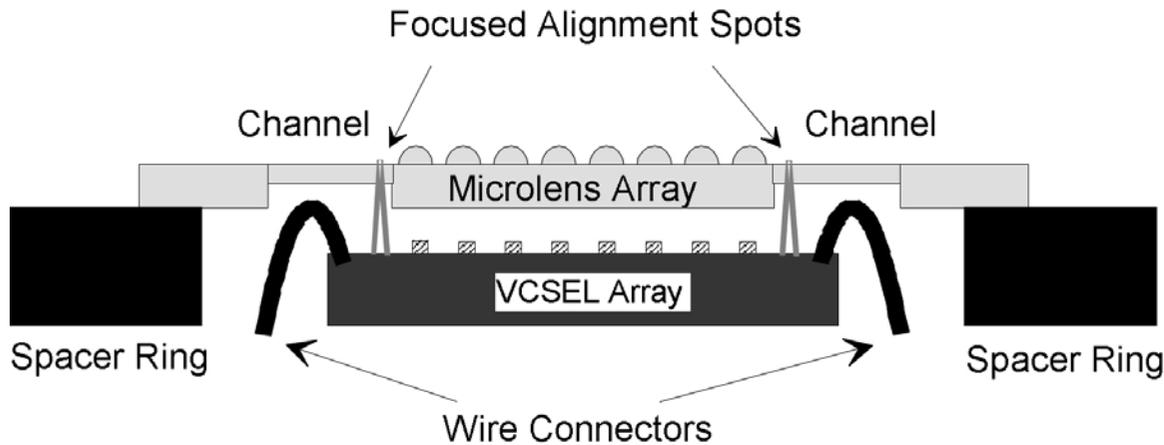
VCSEL Array



- ▶ 8x8 array, grown by MOVPE
- ▶ Strained AlGaAs/GaAs/InGaAs
- ▶ 250 μ m pitch, 10 μ m aperture
- ▶ 2mW, >500Mbit/s, $\lambda=967\pm 0.7$ nm
- ▶ $V_{th} = 1.4$ V, $I_{th} = 0.7$ mA, $\eta = 14\%$

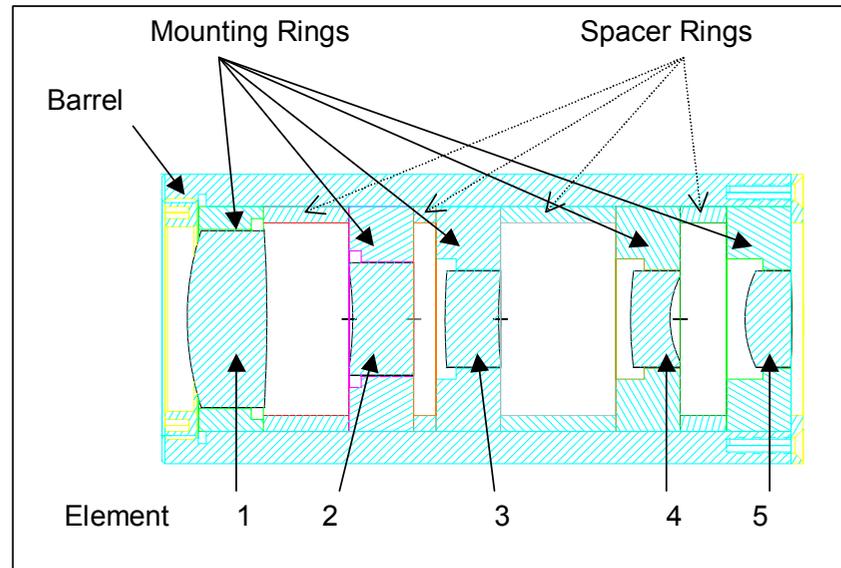
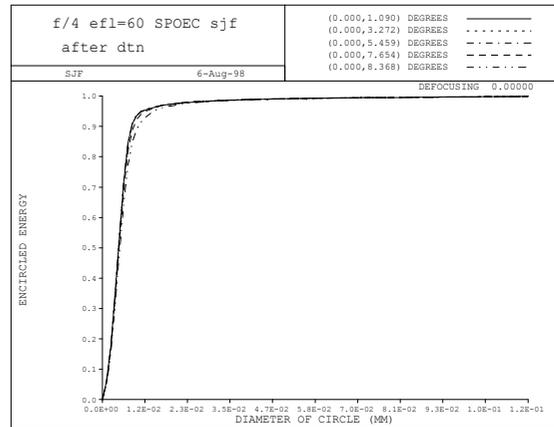
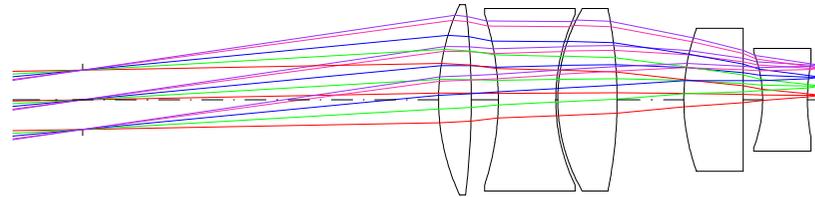


Integration of VCSELs with Microlenses



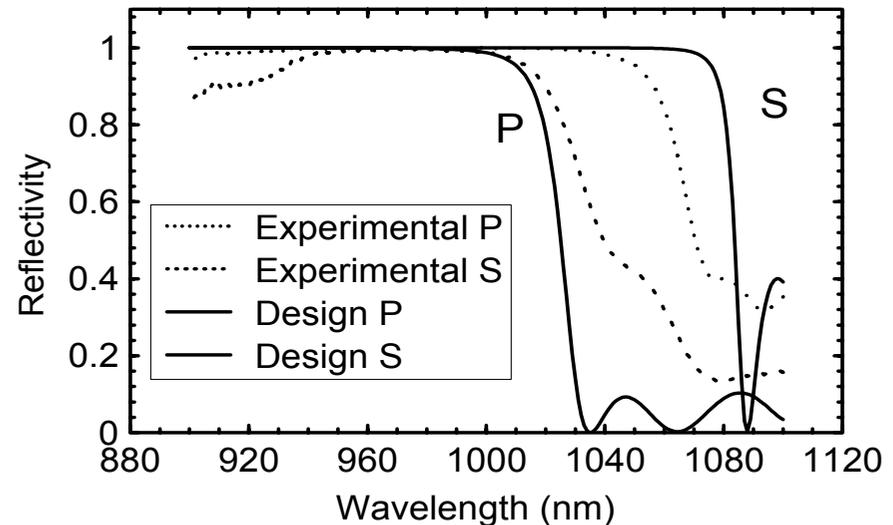
Bulk Optics

- ▶ Telecentric Image Relay
- ▶ Custom Designed Lenses
- ▶ Field Sizes up to 17.5mm
- ▶ Detectors/Modulators $35\mu\text{m}$
- ▶ 960nm and 1047nm
- ▶ $10\mu\text{m}$, 1 arcmin tolerances

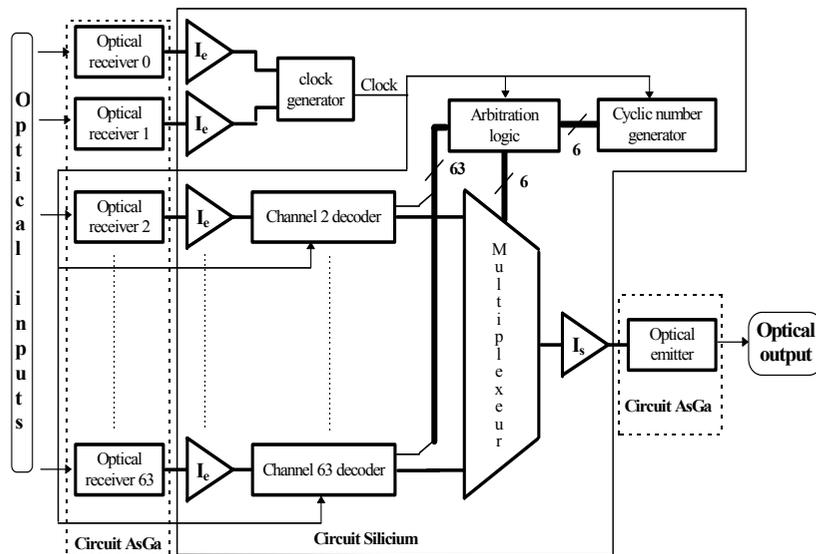


Beam Steering

- ▶ Polarising Beamsplitter over 15 degrees at 1047nm
- ▶ Polarisation independent reflector at 960nm
- ▶ Thin Film Dichroic at 45 degrees on B270
- ▶ 5 μm thick, 27 layers of TiO_2 and SiO_2



Smart Pixels - Silicon CMOS



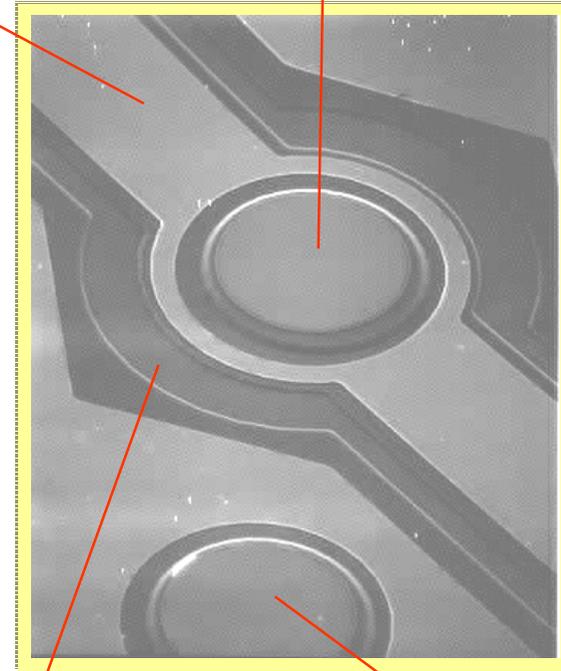
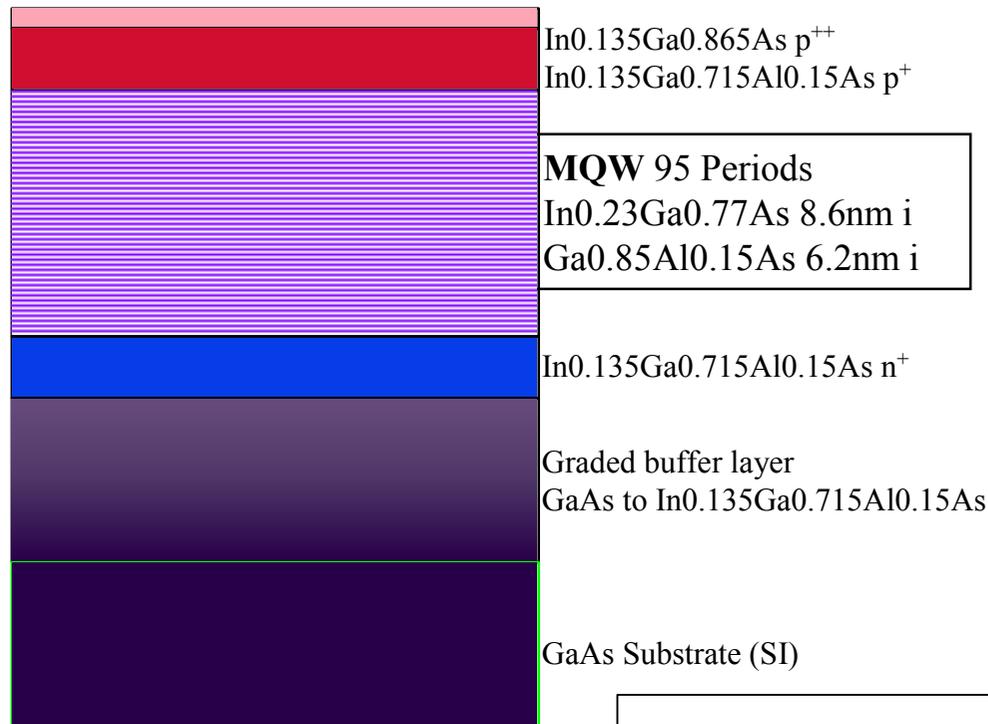
- ▶ 0.6 micron CMOS (AMS)
- ▶ optical clock input
- ▶ header decoding
- ▶ Analogue design
 - sensitivity $5 \mu\text{A}$
 - optical input $\sim 10 \mu\text{W}$
- ▶ Clock receivers based on transconductance-transimpedance amplifier

Forbes and Walker *Electron Lett* 34(6) 1998

Smart Pixels - InGaAs-based devices

n^+ -contact rail
to modulators

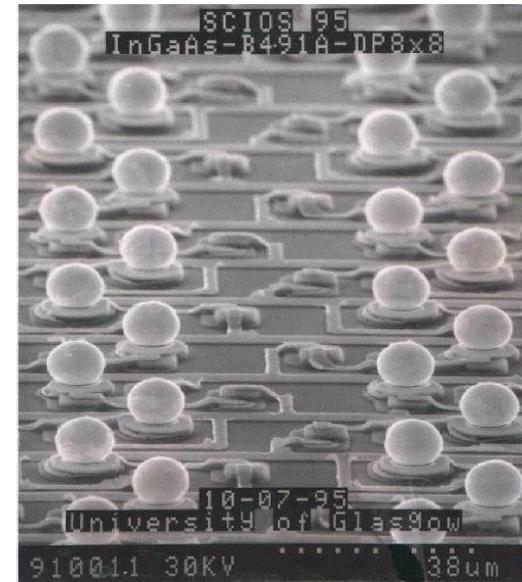
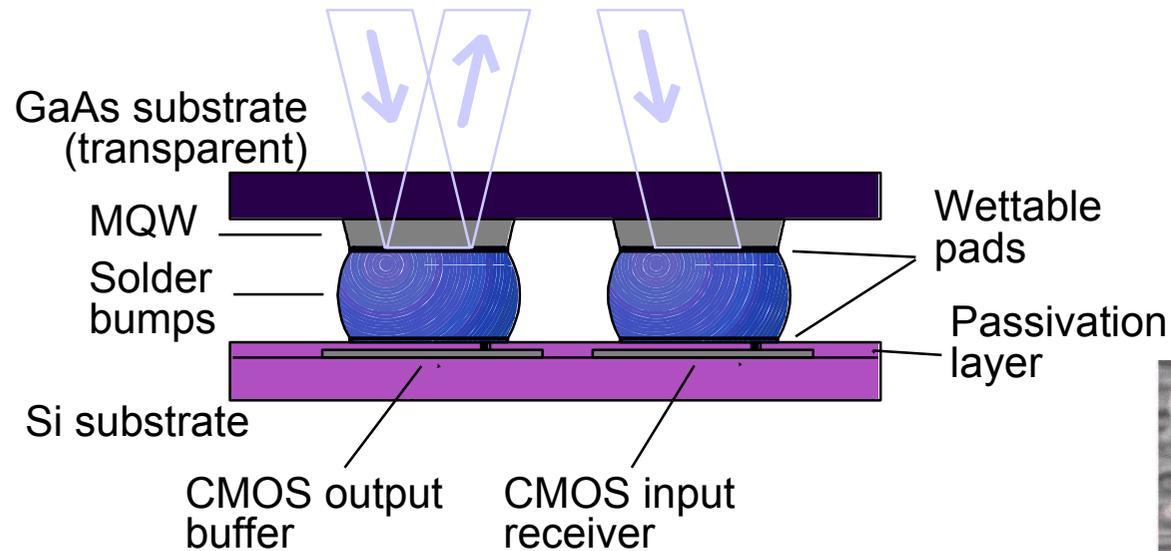
Modulator



Isolation trench

Detector

Flip-Chip Integration

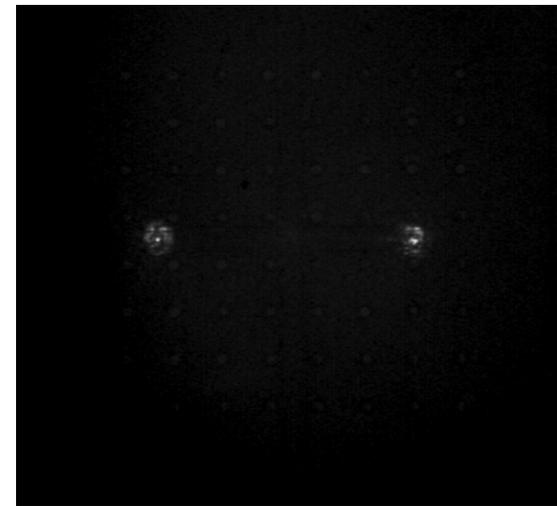


Flip-Chip service provided by

Marconi
Materials Technology

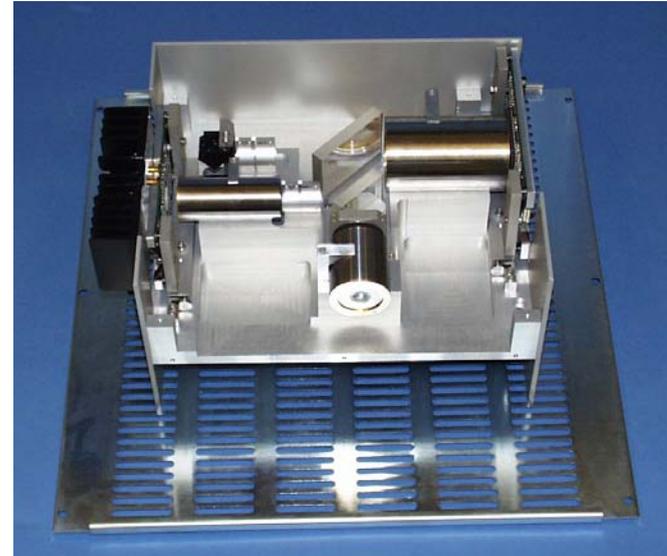
Demonstrator Experimental Progress

- ▶ Demonstrator hardware assembled
- ▶ Assembly of Main Chip a week ago
- ▶ Early electrical test of chip encouraging
- ▶ Rigorous testing in progress
- ▶ Optical beam alignment in progress



Summary

- ▶ SPOEC - A demonstrator test bed for Tbit/s i/o to Si-VLSI
- ▶ Leading edge VCSEL, optical and electrical components
- ▶ Demonstrator assembled
- ▶ Test process begun



Acknowledgements and Further Information

▶ This work is funded by the European Commission as part of ESPRIT MEL-ARI Opto-Cluster, Project 22668 SPOEC



▶ A.C. Walker et al. *IEEE J. Selected Topics in Quant. Electron.* Vol. 5, No. 2, pp 236-249 (1999)

▶ Prof. Andy Walker (A.C.Walker@hw.ac.uk)

▶ <http://www.phy.hw.ac.uk/resrev/SPOEC/index.htm>