Interconnections

1. Introduction

This literature survey will give an overview of electronic interconnect patterns, polymer waveguides and FPGA's.

- Chapter 2 introduces the current interconnect technology of metal tracks and shows that there are 2 distinct domains governing them. It also introduces the fact that they are limited at the maximum speed of signals that can propagate.
- Chapter 3 gives an overview of how processors and memory are actually interconnected using these metal tracks. Some graphs are given at the end showing the performance of different static networks
- Chapter 4 explains the advantages and disadvantages of using optical interconnection and why polymer waveguides have an advantage when used with current PCB technology.
- Chapter 5 is an overview of some fabrication techniques of polymer waveguides
- Chapter 6 shows some of the theory of optical waveguides.
- Chapter 7 lists a few of the structures that can be fabricated in waveguides and the losses associated with them
- Chapter 8 explains the mechanism of hybridising active devices onto a substrate with waveguides.
- Chapter 9 gives a quick runthrough of the mechanics of an FPGA and brings together the ideas in the preceding chapters in an example application of an FPGA.

2. Electronic Interconnects

Traditionally all electronic communication has been over metal wiring whether it is the internal wiring of micrchips or the wiring between these chips across a PCB. There are 2 distinct domains of transmission of signals across wiring that will be discussed, namely transmission lines and those that are RC limited. This chapter will conclude with a discussion of the bandwidth limitations of both these circuits.

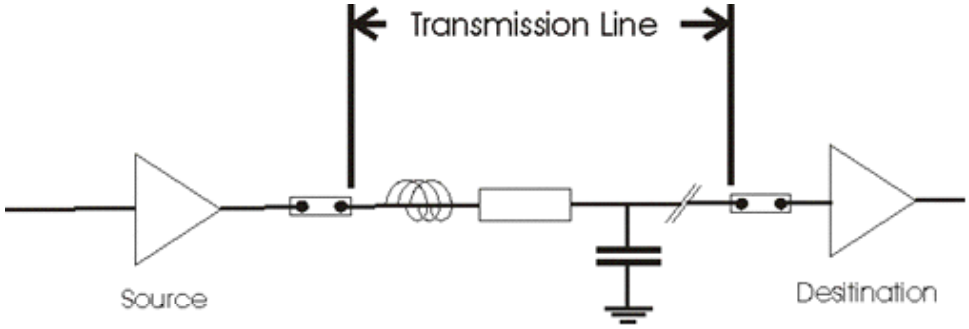
2.1. Transmission Line

[1], [2] For a varying electrical signal the electrical path is considered to be a transmission line when:

$$l >> \frac{v \cdot t_r}{\sqrt{\varepsilon_{eff}}}$$

where v is the velocity of the signal in the transmission medium (~ 20cm per nanosecond for the copper wiretypically used on PCB's), t_r is the rise time and ε_{eff} is the relative dielectric constant of the media (~ 3.5 for PCB). Electrical paths on PCB can be considered to be transmission lines when the track length is greater than a few cm's.

With a transmission line, normal circuit theory is can no longer be used. This is due to the energy stored in the reactive components along the line. The diagram below shows how a transmission line is modelled.



The impedance of such a line is given by:

$$Z_l = \sqrt{\frac{R_l + j2\pi f L_l}{j2\pi f C_l}}$$

where the resistance, capacitance and inductance are per unit length and f is the frequency of the system to be considered. For this reason transmission lines are sometimes referred to as LC limited.

If the resistance can be approximated to zero, there is an impedance of

$$Z_l = \sqrt{\frac{L_l}{C_l}}$$

The velocity with which a signal can travel is then given by:

$$v = \frac{1}{\sqrt{L_i C_i}}$$

The next consideration of transmission lines is reflections. If the impedance is not matched at the end of line then the wave being transmitted can be reflected. This has a direct analogue with AR coatings in optics but here is called impedance mismatch. For a sinusoidal wave with an open output the wave will be 100% reflected and a standing wave will be created in the transmission line. There will be resonance when the length of the line is λ/2, λ, 3λ/2 etc. When the impedance is mismatched but not shorted there will be less reflected ie less loss. This mis-matching can occur at 2 points in a transmission line both of which must be considered: when the line is terminated by a resistive load and when 2 transmission lines are joined.
The details of the fabrication of such transmission lines on PCB are given by [3]. A particular problem with transmission lines on PCB are via holes. These disrupt the electrical path by causing a signal delay due to their inductance and capacitance. Modelling and experimental results are given by [4], [5], [6].
The final word here on transmission lines should be that the speed of these transmission lines on PCB is much less than the clock rate of chips [13]. This is due to loss, crosstalk and wave reflection. Intelligent layout of chips on PCB and different PCB materials are possible solutions, however chapter 4 will introduce an optical interconnect alternative.

2.2. On Chip Interconnections

The connections within a chip are not in the transmission line domain. These connection are said to be RC limited and governed by the laws of simple electrical circuits. The resistance and capacitance is dictated by choice of material, geometry and size of circuit. [7], [12] discusses the current situation and problems that will occur as feature size on chip decreases.
With decreased feature size the signal delay for local connections between features will decrease. But for on chip global connections, the RC delay will start to drastically effect the performance of the chip. Currently this has been solved with lower resisitivity metal connections (copper), lower dielectric material between connections and by improved routing of interconnects [11], [12]. Future solutions could include optical interconnections, which will be discussed in chapter 4, the use of RF either by waveguides or free space across chip [7], [12] and by 3D integrated circuits [8], [9], [12].

2.3. Bandwidth Limitations

The bandwidth for all for all electrical interconnections [13] is given by:

$$B_{\max} \approx B_0 \frac{A}{l^2}$$

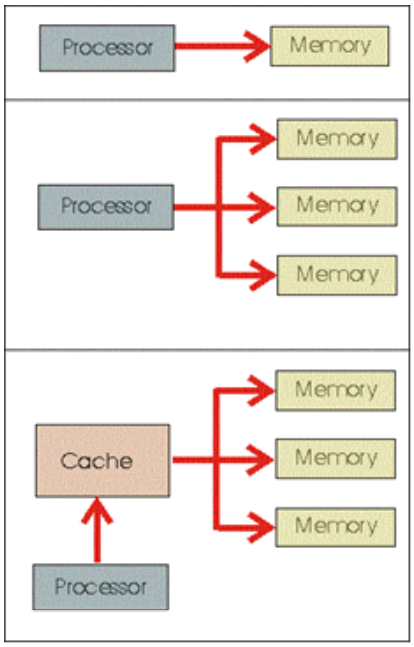
For off chip lines ie. LC limited transmission lines B_o is ~ 10^{15}. For on chip ie RC limited lines B_o is ~ 10^{16}.
The ratio A/l^2 is fixed by the architecture of the system being designed. For a given architecture it is known how many wires will be needed and how far those wires will need to travel. By the very nature of the above equation increasing or decreasing the scale of the system does not solve any problems. An example is the wiring problem on chip even though it is small with short wires.

3. Interconnect Patterns

This chapter will talk about the interconnections at an intra and inter board level [14], [15]. Ideally the bandwidth of a system should only be a product of processor, memory and interconnection bandwidth the interconnection bandwidth being dealt with in the last section. However as shall be illustrated in this chapter the architecture also effects the bandwidth of a given system.
The case of a single processor will be illustrated first with parallel processor patterns given following this. Several types of network will be given and the characteristics of some of these then graphed.

3.1. Serial Computer or Uniprocessor

The serial computer can be classified as SISD (Single Instruction Stream, Single Data Stream). The serial computer is cheap and easy to implement. The speed is limited by execution rate of instructions and the speed at which data is exchanged between CPU and memory. The speed of memory exchange rate can be increased by dividing memory into memory banks. This is called memory interleaving and can also be increased by using a buffer between the slow main memory. This fast memory is called cache memory. The principle behind this memory is that if a word is accessed from memory, subsequent memory accesses will be from words in the neighbourhood of that memory location. One further improvement to the speed of serial compuers is to fetch the next instruction while executing the current instruction. This is called instruction pipelining.

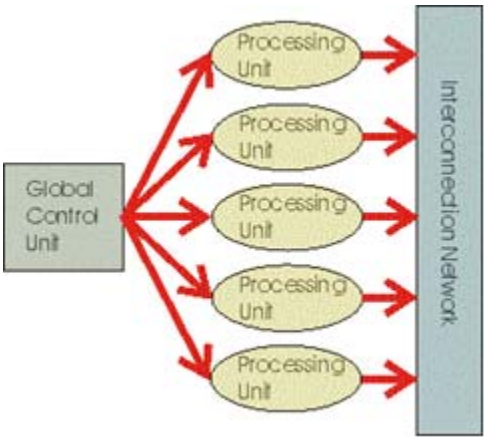


3.2. Parallel Computer

Parallel computing can be split into 2 architectures, SIMD (single instruction stream, multiple data stream) and MIMD (multiple instruction stream, multiple data).

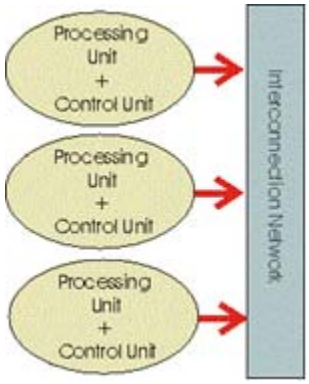
- SIMD

Many of the early parallel computers were of this type. The same instruction is executed synchronoulsy by each of the multiple processors. Each processor also has its own memory indicated in the diagram by the processing unit block. Controlling the system is a global control unit. SIMD's do not use off the shelf parts.



- MIMD

MIMD is the popular implementation of parallel computer due to 2 reasons. MIMD's are flexible as they can either be set up to focus on one application or to run many tasks simultaneously. They can also be cheap to implement by using off the shelf parts. In a MIMD system each processor is capable of executing a different program independent of the other processors.



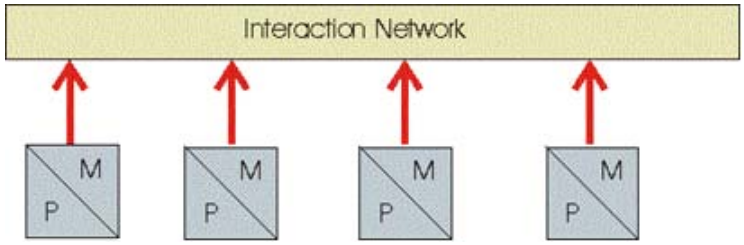
- Comparison of SIMD and MIMD

SIMD computers require less hardware thean MIMD computers as there is only one global control unit. Less memory also needed as only one copy of program needed. However different processors cannot execute differect instructions in the same clock cycle. Lastly for a SIMD the processor must be specially designed.
MIMD computers store the program and operating system at each processor and most importantly can use off the shelf processors A MIMD system can also be operated in SIMD mode with extra hardware for fast synchronisation. For these reasons MIMD systems are the favoured approach for parallel computing and will be the implementation discussed here.

3.3. Processor Interaction

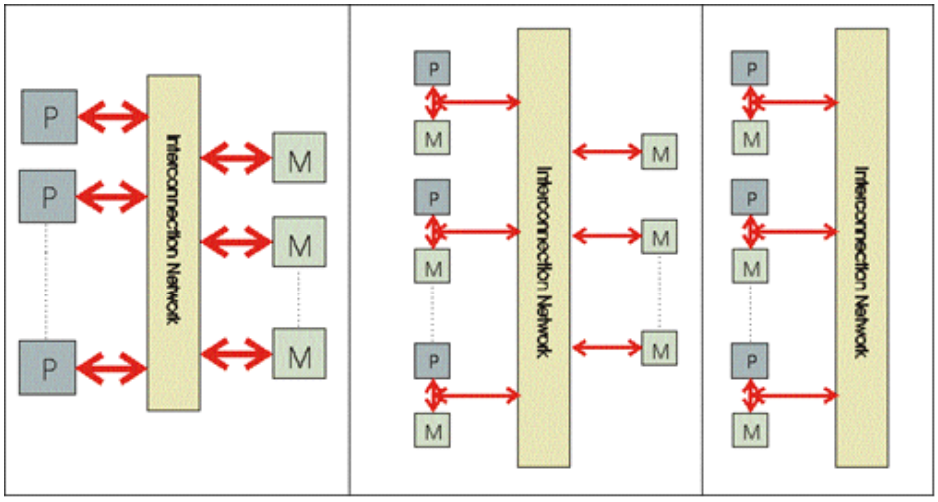
MIMD's can fall into 2 classes depending on the memory organisation.

- Message-Passing Architecture



Each processor has its own local memory. MIMD's of this type ae often called multi-computers. They can be on the same PCB or can use a LAN but for either type a high bandwidth interconnect is needed. This architecture is cost effective if most memory access is to local memory. As memory is local the system can be optimised for low memory latency.

- Shared Address Space Architecture



This architecture supports read and write access by all processors to a shared address space. MIMDs of this type are often called multi-processors. For this to be viable the interconnection must have a large bandwidth because during each instruction cycle each processor may need to access a word from the shared memory through the interconnection network UMA (uniform memory access). Extensions to this idea could be local memory and a global memory or only using local memory NUMA(non uniform memory access). Each can include cache for speed. With this architecture there can be a problem of cache coherence. This is when the value in cache is different from that in shared memory.

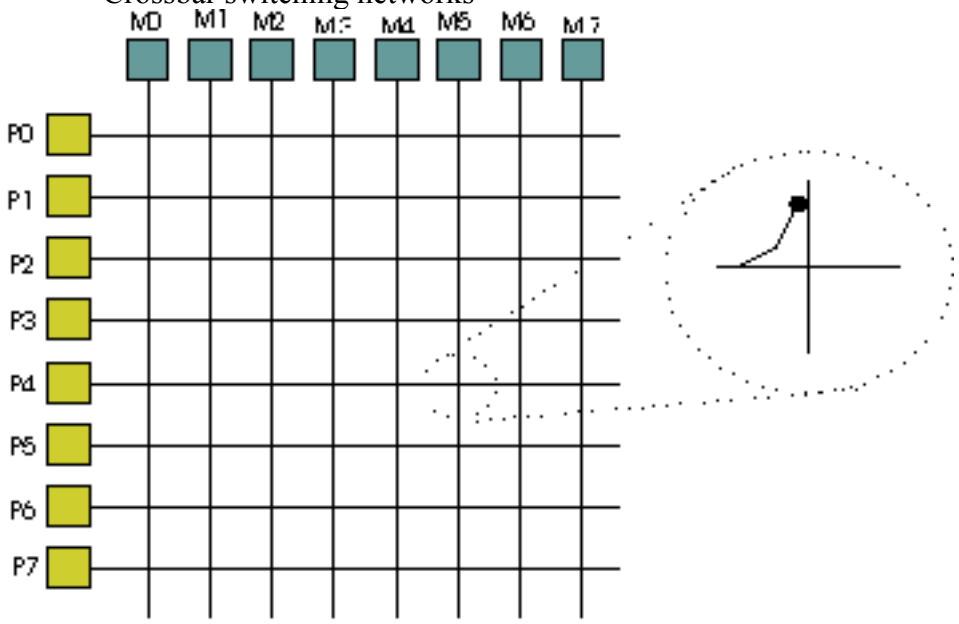
3.4. Types of Network

Networks can either be static or dynamic.

- Static – point to pint links between processors. Also called direct networks. These are usually for message passing computers.
- Dynamic – built using switches and communication links. Communication links are connected dynamically with switches. Also called indirect link. Usually for shared address space computers.

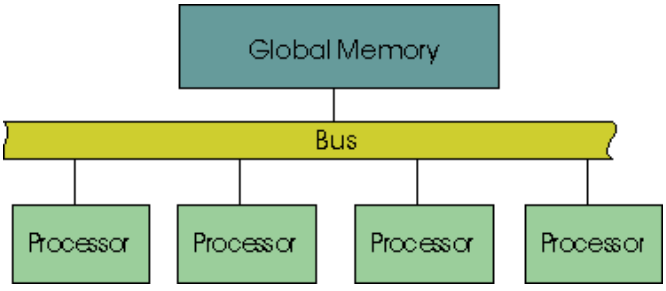
3.5. Dynamic Interconnection Networks

- Crossbar switching networks



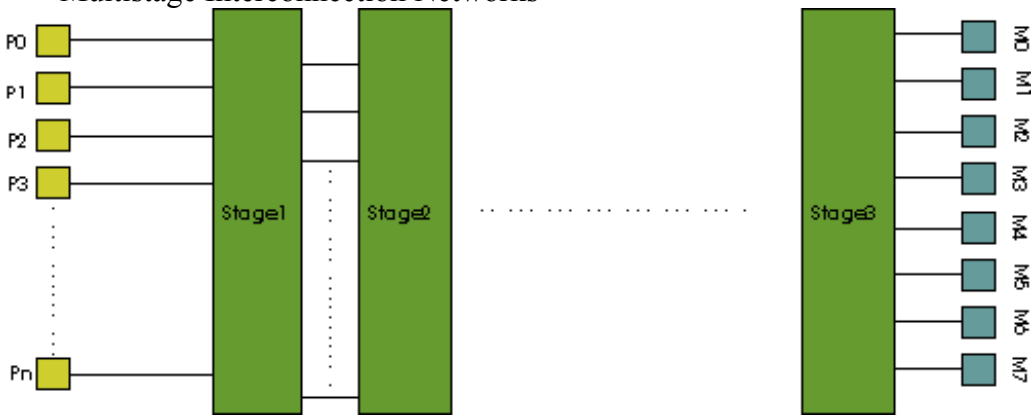
This consists of a grid of switching elements so that any processor can access any memory bank. The number of memory banks must be at least equal to the amount of processors otherwise some processors may not be able to access any memory. As the amount of processors becomes large, the switching network becomes unpractical due to the size of the switching network required.

- Bus-based networks



Due to the simplicity of design this network appears attractive. However for a low bandwidth bus there may be processors left waiting to access the memory.

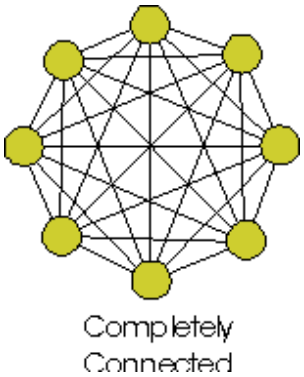
- Multistage Interconnection Networks



This network is somewhere between the performance of the crossbar and the bus. It is more scalable than the bus in terms of performance and more scalable than the crossbar in terms of cost to implement.

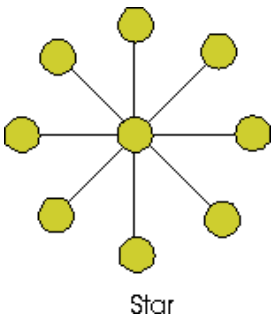
3.6. Static Networks

Completely Connected



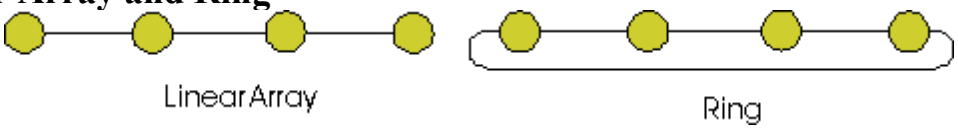
This network is ideal in terms of performance as each processor is connected to each other by a single step.

Star



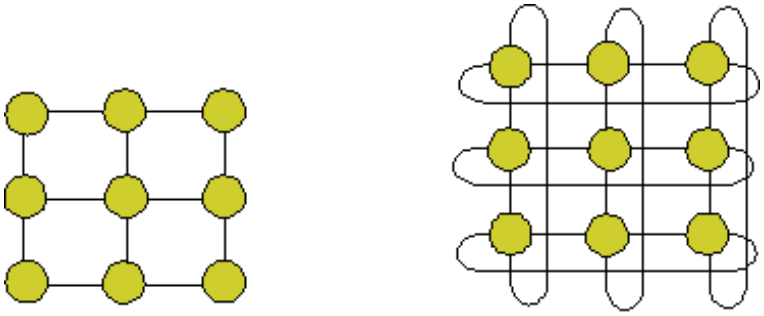
In the star network there is a single processor that links all the others. This can be compared to the bus network. The central processor is the bottleneck in this processor.

Linear Array and Ring



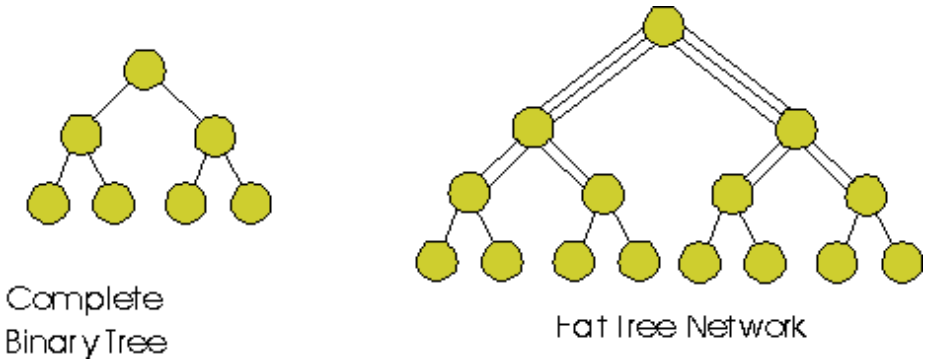
The linear array is a simple way of connecting processors. The ring topology builds on this idea.

Mesh



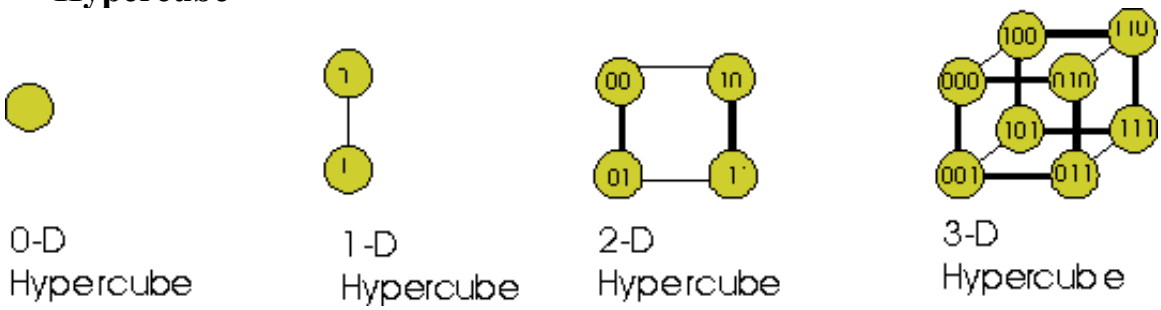
The mesh is an extension of the linear array to 2 dimensions. Each processor has a direct link to four other processors. For extra connectivity the processors at the edge can be connected by wraparound connections.

Tree



In the tree network there is only one path between any pair of processors. Linear array and star network are special cases of tree network. At higher levels of the tree there is a communication bottleneck This can be solved by adding extra links higher in the tree.

Hypercube



A hypercube is a multidimensional mesh of processors with exactly 2 processors in each dimension. The binary representation of each processor is included in the diagrams above. Each processor is connected to another only if there binary representations differ by only one bit position. In a d-dimensional hypecube each processor is connected to d other processors. Other parameters are given in [14].

k-ary, d-cube

d-dimensional hypercubes are also called binary d-cubes. This can also be described as a d-dimensional mesh with 2 processors along each dimension.

A ring network is a 1-dimensional structure with p-processors along the only dimension.

Both of these are at the extreme of a type of network called k-ary, d-cubes. d is the dimension and k is the radix, which is the number of processors along each dimension.

3.7. Characteristics of Various Static Network Topologies

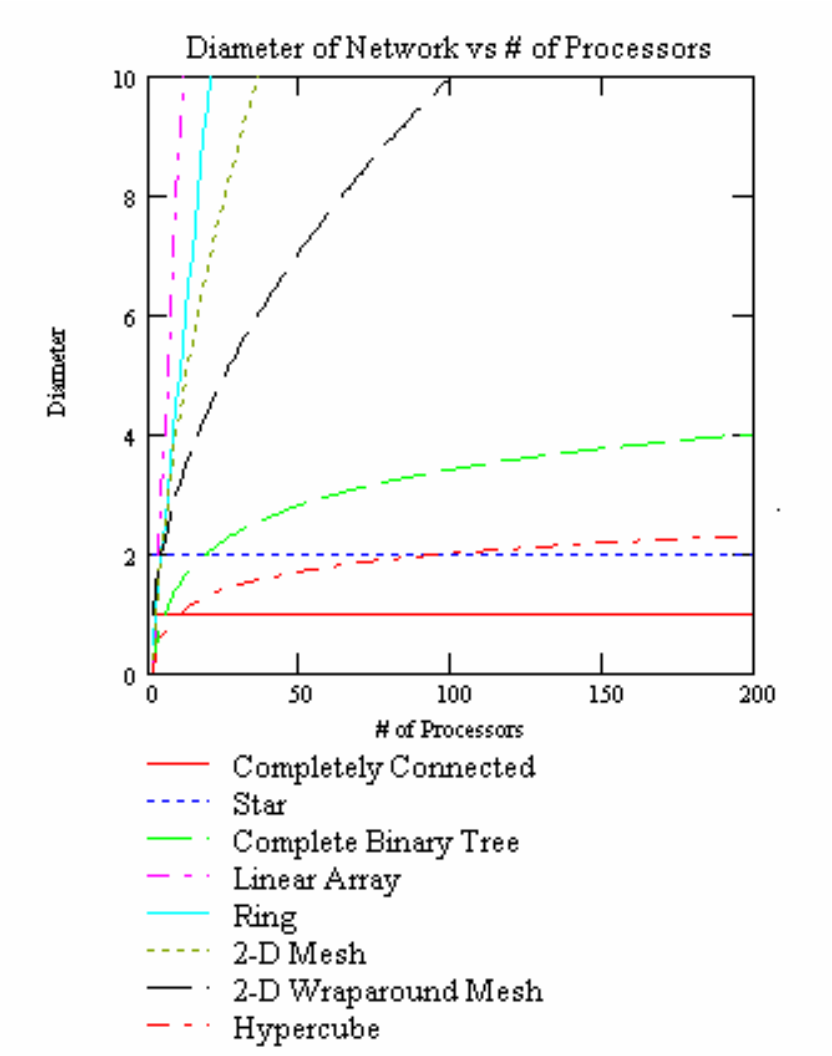
- Diameter – Maximum distance between any 2 processors. Chapter 2 discussed the need for short electrical interconnection length to increase bandwidth.
- Arc Connectivity – High connectivity is desirable as this avoids contention for communication resources. Arc connectivity is the minimum number of arcs that must be removed to break a network into 2 distinct networks.
- Bisection Width – Minimum number of links that must be removed to partition the network into 2 distinct halves. The *channel width* is the number of bits that can be communicated simultaneously over a link connecting 2 processors which is equal to the number of physical wires in each communication link. The *channel rate* is the peak rate at which bits can be communicated over a single wire. *Channel bandwidth* is the product of channel rate and channel width. *Bisection bandwidth* is the maximum volume of communication between 2 halves of the network and is the product of bisection width and channel bandwidth.
- # of Links – Number of links required by a network.

Network	Diameter	Bisection Width	Arc Connectivity	# of Links
Completely Connected	1		p-1	p(p – 1) / 2
Star	2	1	1	p - 1
Complete Binary Tree	$2 \cdot \log((p+1)/2)$	1	1	p - 1
Linear Array	p-1	1	1	p - 1
Ring	p / 2	2	2	p
2-D Mesh	$2(\sqrt{p}-1)$	$\sqrt{p}$	2	$2(p-\sqrt{p})$
2-D Wraparound Mesh	$2(\sqrt{p}/2)$	$2\sqrt{p}$	4	2p
Hypercube	log p	p/2	log p	(p log p) / 2

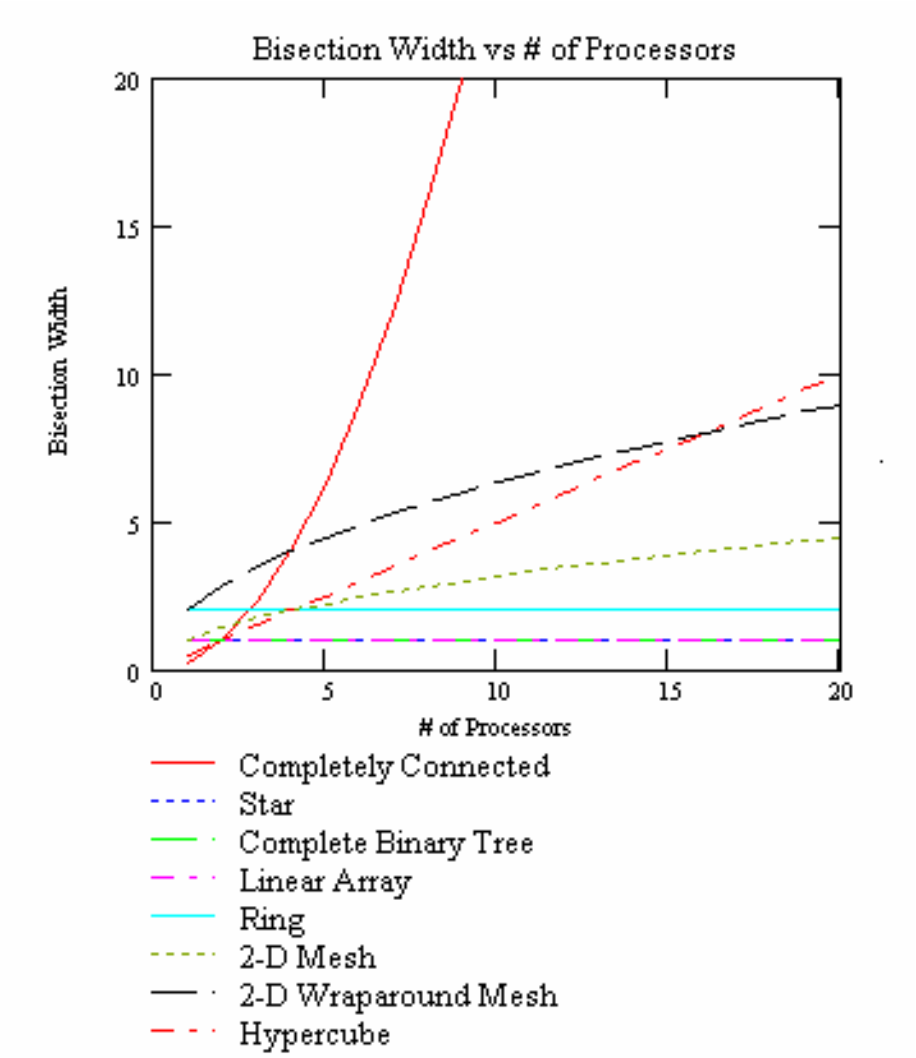
3.8. Performance of Various Static Network Topologies

Below are 4 graphs for each of the metrics defined in the last section. This graphically shows that depending on the constraints and what is needed from a system dictates what topology is chosen.

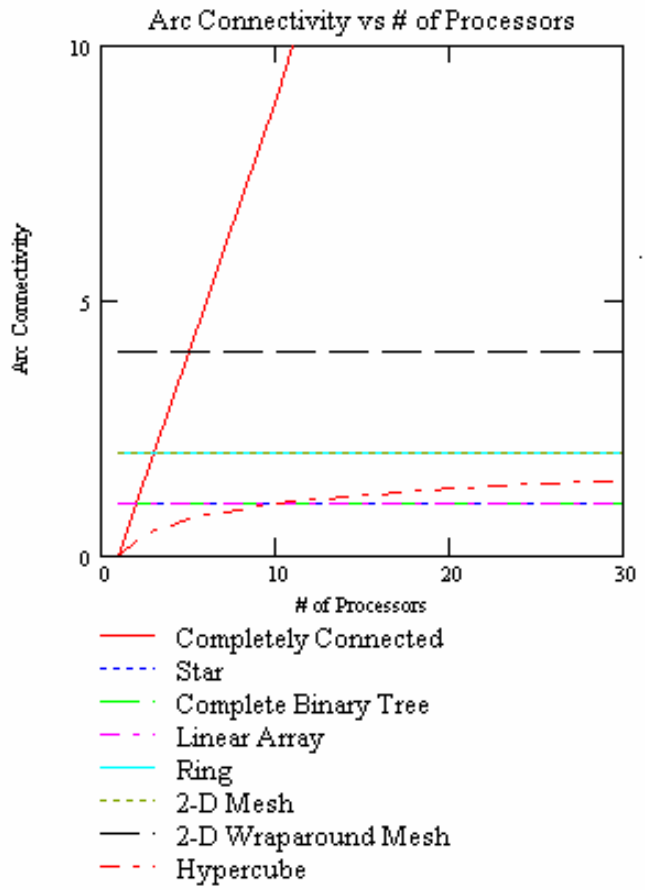
Diameter of Network vs Number of Processors



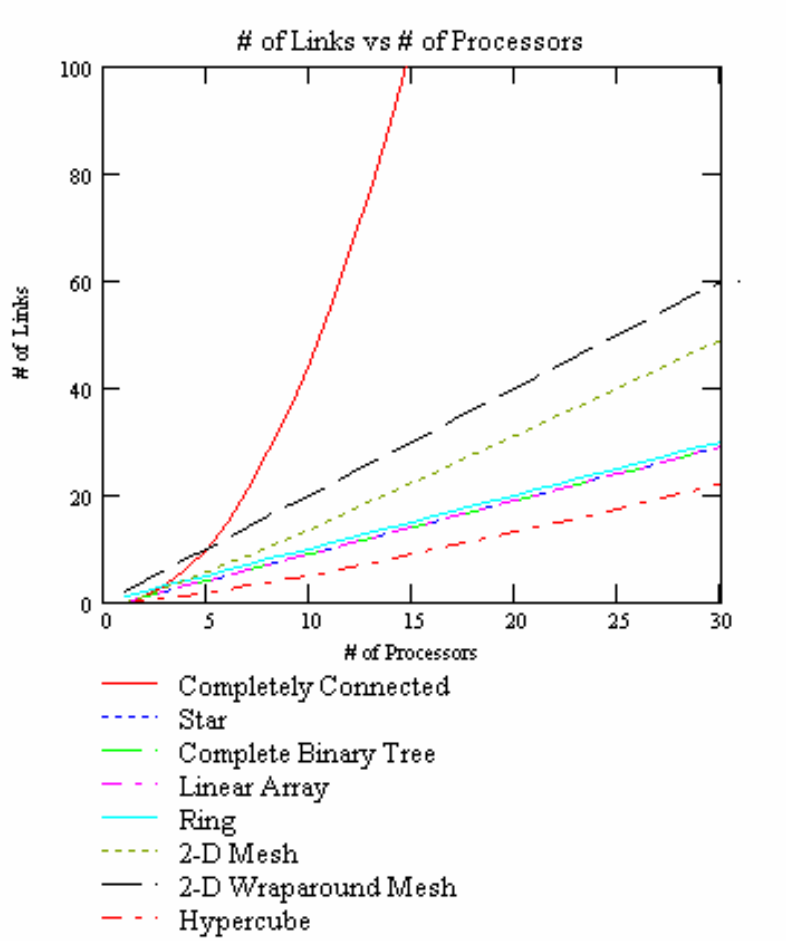
Bisection Width vs Number of Processors



Arc Connectivity vs Number of Processors



Number of Links vs Number of Processors



4. Optical Interconnections

This chapter will show the need for optical interconnections and where they will be implemented. Polymer waveguides will be introduced and the characteristics of some commercially availably waveguides listed.

[7], [12], [13], [16] all discuss the need for an interconnect in which the bandwidth is not constrained in the same way as electrical signals over metal tracks. As discussed in chapter 2 resistance, capacitance and inductance limit the signal speed. It will be increasingly difficult to achieve higher speeds over metal tracks with these constraints at all levels of interconnect.

4.1. Advantages and Disadvantages

Optical interconnect advantages [7, 13]

- Higher bandwidth than possible with metal tracks
- No need for hierarchy of memory and off chip connections as all optical interconnects will have similar bandwidths and latencies
- Frequency independence. The carrier frequency of optics is ~10^{15}Hz so there is no degradation in the propagation of signals as the modulation frequency is increased because the modulation frequency is negligible compared to the carrier frequency.
- Reduction of power dissipation in interconnects
- Voltage isolation between different parts of the system.
- Density of interconnections
- Surface normal connections. Improves the density of connection available as well as taking signals directly to the chip rather than through it. This also improves latency.

Optical interconnect disadvantages [7, 13]

- Currently not possible to monolithically integrate laser with silicon device
- Extra level of hybridisation / fabrication.
- Large size and number of components to be hybridised / fabricated. This includes laser drivers, lasers, photodiodes, photodiode circuitry and waveguides.
- Power dissipation of extra components

4.2. Optical Interconnection

If optical interconnects are to be used they can be used in 3 domains for interconnection of computers.

- Board to Board: The reach here is of the order 1m as an optical backplane for interconnections between computers. [17] illustrates a timeline and states that these could be commercially available within 2 – 5 years. Companies currently involved with this include Primarion[18], Optical Crosslinks and Daimler Chrysler [19]. The optical backplane can be implemented in many ways including free space [20] waveguide [21], and fibre optics.

- Chip to Chip: The reach is of the order 0.1m. These interconnections are inside the computer itself and link individual chips. [17] illustrates a timeline and states that these could be commercially available within 5 - 10 years. These interconnections will probably be a waveguide.

- On Chip: The reach here is <<0.01m. These interconnections are on the chip itself and as [17] illustrates will be for on chip global interconnection. Again [17] shows the timeline for this. This would be the most difficult interconnection to achieve optically.

4.3. Polymer Waveguide

Polymer waveguides are one possible solution for implementing an optical interconnection [22], [23], [24]. The main advantage with using polymer waveguides is that the fabrication process is compatible with current PCB technology so would be suitable for chip to chip connections. The optical loss of such guides is at a minimum at the datacomm wavelength of 850nm. Single mode and multimode waveguides have been fabricated as have several passive structures such as splitters.

Below are some polymer materials available for waveguides.

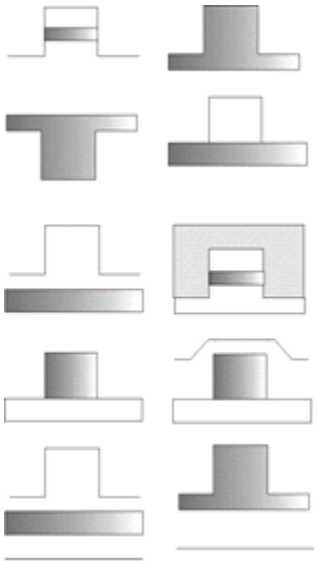
Manufacturer	Polymer Type	Patterning Techniques	Optical Loss dB/cm @ 850nm
Allied Signal	Acrylate	Photoexposure / wet etch, RIE, laser ablation	~0.02
	Halogenated Acrylate	Photoexposure / wet etch, RIE, laser ablation	~<0.01
Amococ	Fluorinated Polyimide	Photoexposure / wet etch	?
Dow Chemical	Benzocyclobutene	RIE	?
	Perfluorocyclobutene	Photoexposure / wet etch	?
DuPont	Acrylate	Photolocking	~0.18
General Electric	Polyetherimide	RIE, laser ablation	~0.24
Hoescht Celanese	PMMA copolymer	Photobleaching	?
JDS Uniphase	BeamBox	RIE	?
NTT	Halogenated Acrylate	RIE	~0.02
	Deuterated Polysiloxane	RIE	?
	Fluorinated Polyimide	RIE	?

5. Fabrication

This chapter will show some fabrication techniques for polymer wavguides that are compatible with existing PCB technology.

5.1. Waveguide Structures

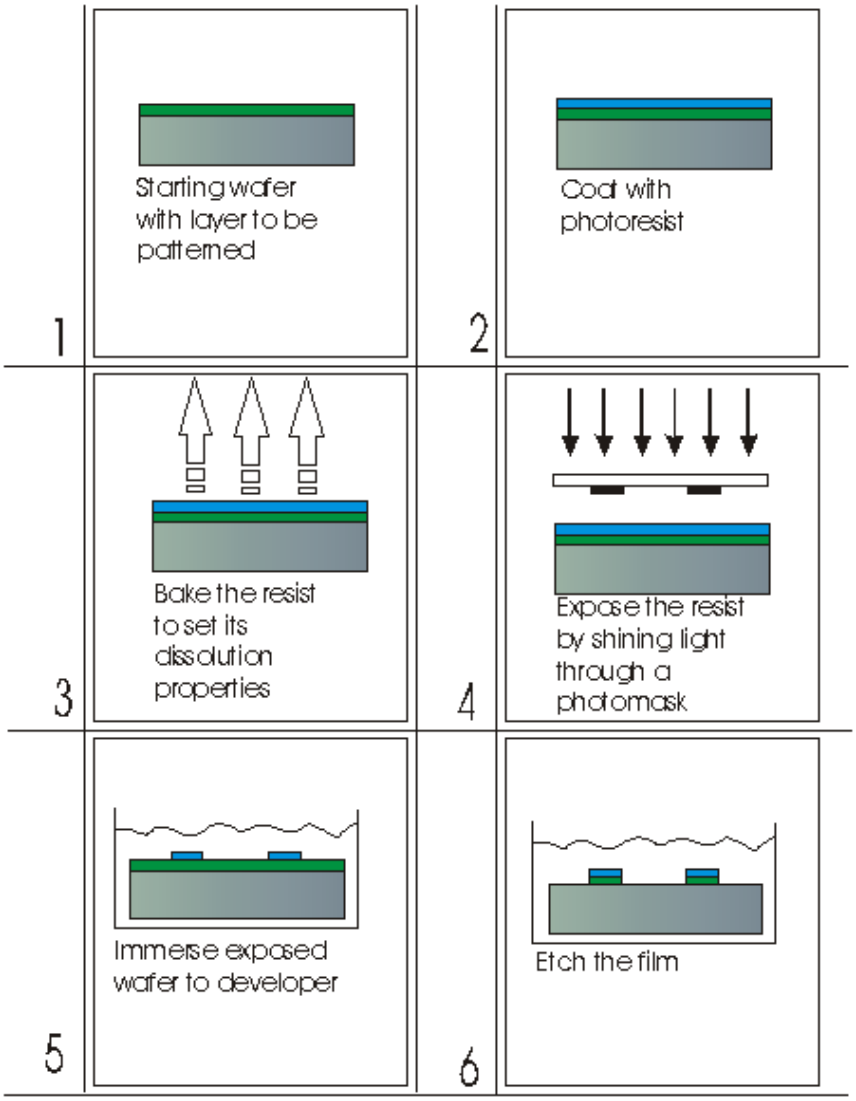
There are many different waveguide structures possible for confining launched light all relying on a refractive index change around the core where the light should be confined. A few of these are shown below [32].



The grey area shows where the region where the light is being guided. The structures can be formed in all standard substrates by etching, doping and growing. The following sections will concentrate on a rib waveguide.

5.2. Standard Fabrication Techniques

The fabrication of waveguides and electronic structures in general is usually a problem of the creation of a 3D structure from a 2D masks [25].
The basics can be distilled down to the following diagrams.

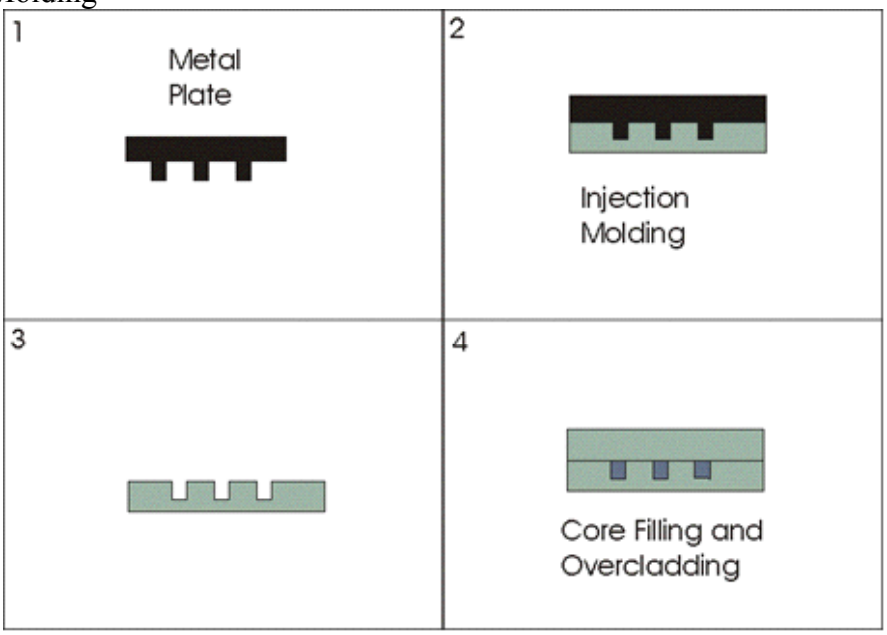


Other techniques have also been developed unique to polymer waveguides, which will now be discussed.

5.3. Embossing and Molding

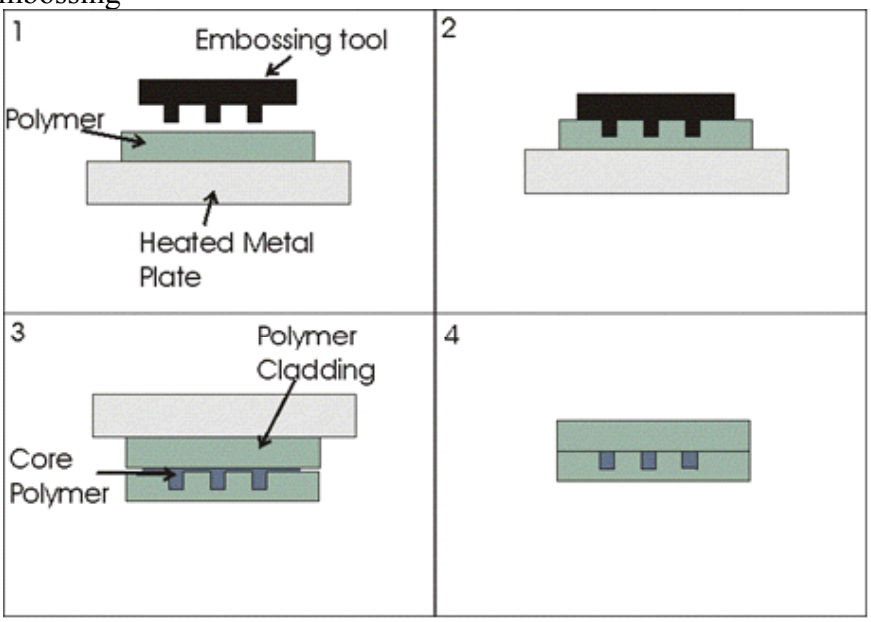
[26], [27], [28] all describe methods of embossing or molding polymer waveguides. In both cases a UV transparent tool is used. Both of these are regarded to be low cost techniques.

- Molding



[26], [28] shows a buried waveguide by the injection molding technique. A metal imprint of the waveguides is transferred to an injection molding machine. The metal is removed and the waveguide structure is defined by grooves. The grooves are then filled by polymer to create the waveguide core. A polymer plate is then pressed onto the waveguides. This removes any excess liquid and protects the waveguides. The waveguides are then cured.

- Embossing

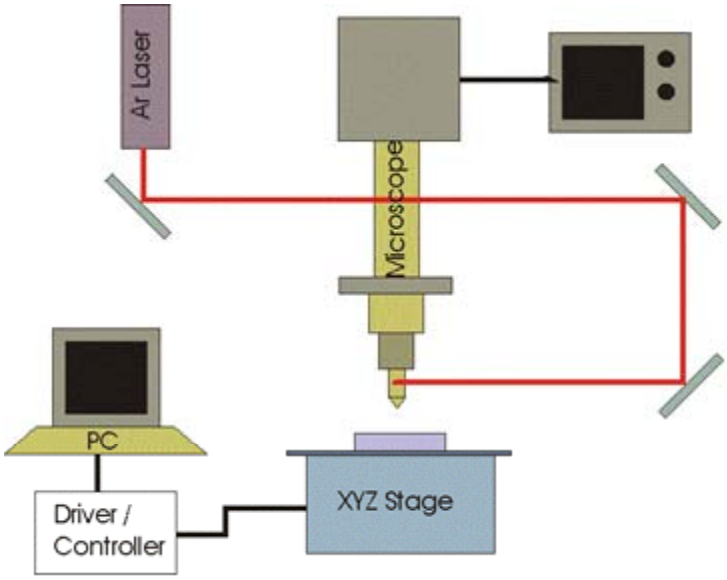


[27] shows an embossing technique for polymer waveguides. A metal masterform is used to emboss the wavguides as grooves into the polymer foil. The grooves are then filled with liquid core polymer, which is hardened and then covered with cladding. The thin polymer foil containing the optical layer is then laminated onto the PCB.

By using these techniques a loss at 850nm of 0.1db/cm has been achieved. This loss is expected to be due to surface roughness. It should be noted that [27] reports an additional 0.15db/cm loss due to the solder reflow process when electrical contact was made. Single mode and multimode waveguides have been created as have 1 x 8 power splitters.

5.4. Laser machining

Laser machining is another novel maskless process [29], [30], [31]. As masks are not created this allows rapid prototyping.



By using this it has been shown that single mode waveguides can accurately be drawn in an acrylate polymer where the size of the mode matches that of optical fibre. The use of this technique has certain advantages. These include being able to write on selected areas without affecting others and being able to write very long structure several metres long if written on rolls of flexible substrate. It is also possible to process substrates with elevated areas, something not possible with contact mask processing.

Using this [29] has reported losses at 840nm of 0.03dB/cm. Bends, y-junctions and couplers were written into acrylate. These were characterised with a good fit between experiment and theory. Finally it was shown that the waveguides drawn were thermally stable at elevated temperatures.

6. Theory and Modelling

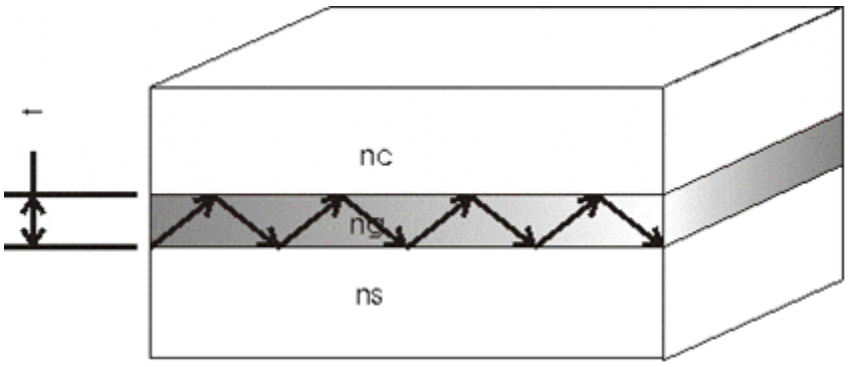
The theory for guided waves will be considered here[32], [33], [34], [35]. Only a slab waveguide will be considered but this is enough to build some physical intuition of the theory of waveguides. The sections will consider single mode, multimode and highly multimode waveguides.

6.1. Single Mode and Multi Mode Waveguide Theory and Modelling

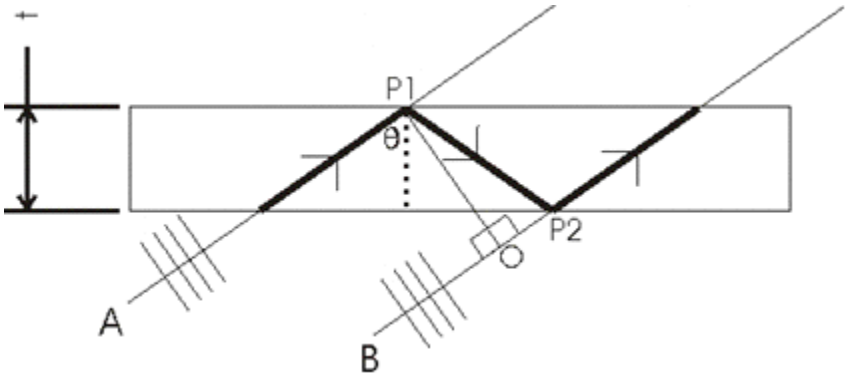
This section will deal with waveguides that are either single or multi mode. A ray optic model will be considered first for a slab waveguide. Although simplistic it allows the number of modes to be calculated and allows physical understanding of the slab waveguide. The more mathematically rigorous electromagnetic model will then be considered. Goos-Hanchen shift will then be discussed which will bring the 2 models together.

6.1.1. Ray Optic Model

This section will determine the number and type of modes as well as the propagation constants and effective indices.
The diagram below shows a slab waveguide that is constrained in the y direction and infinite in the x and z directions. It is assumed for simplicity that at each interface R=1.



By considering this diagram it can be seen that if the wavefronts from A and B are not in phase then destructive interference will occur along the waveguide and the light will no longer propagate.



The condition

$$\Delta L = \overline{P_1P_2} - \overline{P_2O}$$

must then be met for light to propagate through the slab. By trigonometry this can be shown to be:

$$\Delta L = 2t\cos\theta$$

The number of wavelengths in the path length difference is

$$\Delta L / \lambda$$

From this the total phase shift for a wavelength can be shown to be:

$$2\pi\Delta L / \lambda$$

As it is known that each reflection results in a phase shift of π, the condition for A and B to be in phase is given by

$$4\pi t / \lambda \cos\theta - 2\pi = 2m\lambda$$

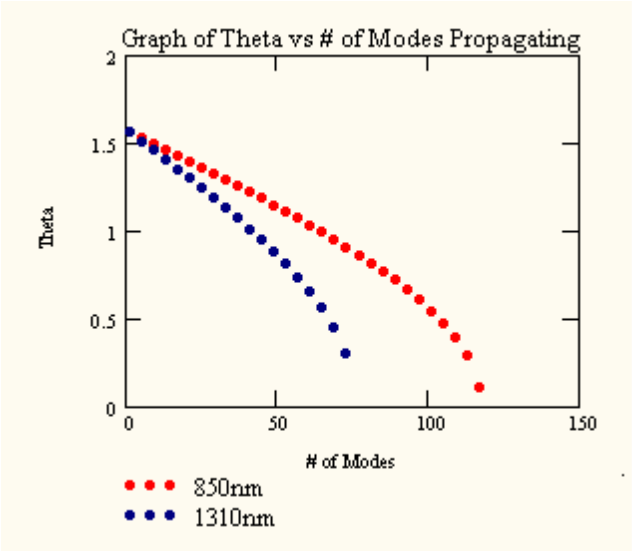
where m is an integer. This can be rearranged to give:

$$\theta_{m`} = \cos^{-1}\left(\frac{\lambda m`}{2t}\right)$$

From the above the condition

$$m` \leq 2t / \lambda$$

must be met. The graph below shows how that the above equation puts a limit on the amount of modes allowed to propagate in the slab waveguide. The curves are for light launched at 850nm and 1310nm. The condition when no mode is allowed to propagate is known as cutoff.



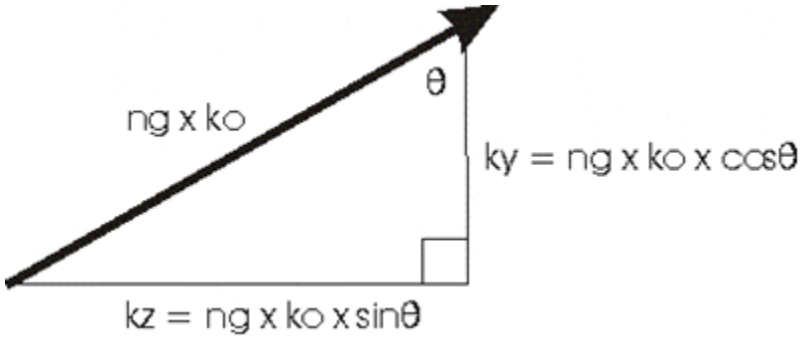
Each mode that is allowed has a propagation constant associated with it. It is known that

$k_0 = 2\pi/\lambda$

and

$k_n = n_g \, 2\pi/\lambda$

where ng is the refractive index of the waveguide. This is in the direction of the wavenormal.



The portion of the propagation constant travelling in the z direction is then calculated by:

$$k_z = k_n \sqrt{1 - \frac{\lambda^2 m`^2}{4t^2}} = k_n \sin\theta_{m`}$$

From this the effective mode index, N, is defined as

$N = n_g \sin\theta_{m`}$

and using this the z directed propagation constant will be redefined as

$\beta \equiv k_z = Nk_0$

This means that the each mode can now be considered as travelling in a straight line down the waveguide with a discrete propagation constant and effective index.
The above can then be continued to accommodate the conditions when the refractive indices are different. The ray optic model allows easy intuition of the situation but is inadequate for accurate modelling. For this the EM model must be used.

6.1.2. Electromagnetic Model

The EM model will allow a determination of the interaction of modes with structures outside the waveguide and for the description of the shape of the mode. The last point will allow calculation of coupling losses. In the last section perfect reflection was assumed (R=1). This is not the case and there is some penetration of the wave into the next media.
As given by [35] the guided modes have the form

$\psi = \psi(x,y)\exp(-j(\omega t - \beta z))$

For the TE modes E_z is zero and satisfy the equation

$$\frac{d^2E_y}{dx^2} + \left[\frac{\omega^2 n^2(x)}{c^2} - \beta^2\right]E_y = 0$$

where

$n^2(x) = n_1^2$ for -d < x < d

$n^2(x) = n_2^2$ for x < -d and x > d

Now

$E_y, H_z and \frac{\partial^2 E_y}{\partial x}$ are continuous at x = ± d

In the guide layer there is:

$$\frac{d^2E_y}{dx^2} + \left[\frac{\omega^2 n_1^2(x)}{c^2} - \beta^2\right]E_y = \frac{d^2E_y}{dx^2} + u^2E_y = 0$$

In the confining layer there is:

$$\frac{d^2E_y}{dx^2} + \left[\beta^2 - \frac{\omega^2 n_2^2(x)}{c^2}\right]E_y = \frac{d^2E_y}{dx^2} + w^2E_y = 0$$

where in the above

$$u^2 = \omega^2 n_1^2 / c^2 - \beta^2 = \beta_1^2 - \beta^2$$

and

$$w^2 = \beta^2 - \omega^2 n_2^2 / c^2 = \beta^2 - \beta_2^2$$

From this it can be seen that for a wave to be guided the following condition must be met.

$$\beta_1^2 = \omega^2 n_1^2 / c^2 > \beta^2 > \omega^2 n_2^2 / c^2 = \beta_2^2$$

As this allows the guiding layer to have a complex therefore oscillatory solution while the solution in the other layers will be real and exponentially decaying.
The electric field distributions then take the form

$$E_y(x) = E_s \cos(ux)$$

or

$$E_y(x) = E_a \sin(ux)$$

for

$$|x| < d$$

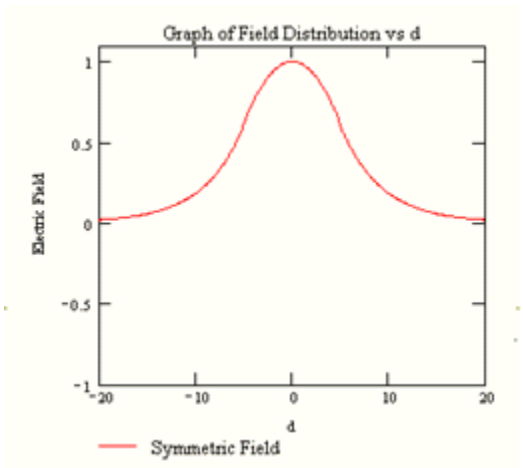
and

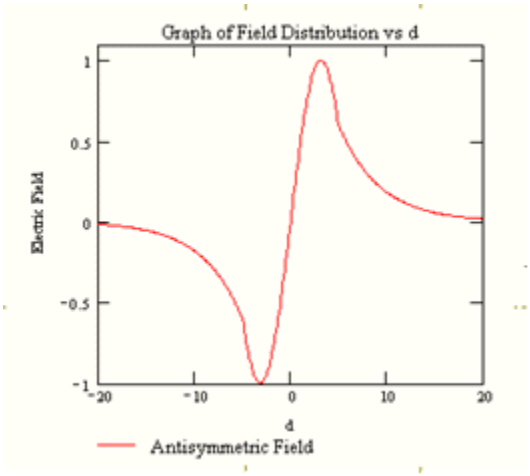
$$E_y(x) = E_a \exp(-|wx|)$$

for

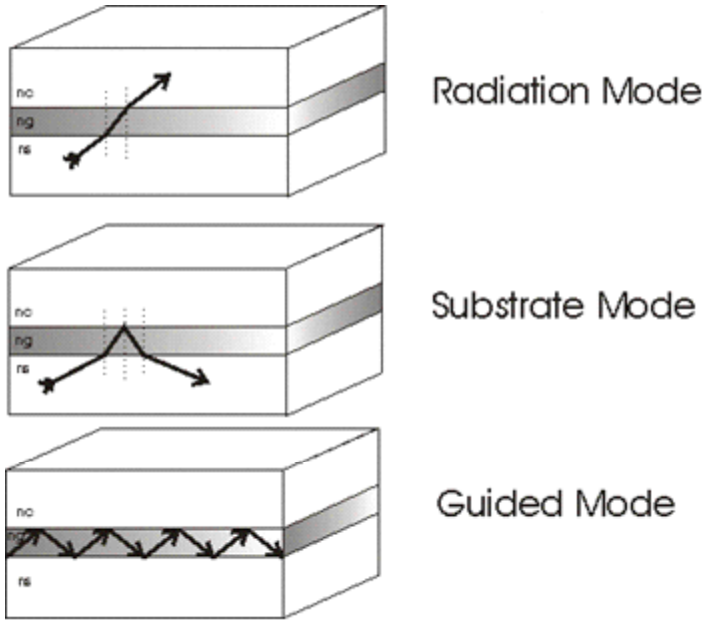
$$|x| > d$$

This shows that in the guiding layer the mode field pattern can either be symmetric or antisymmetric.
The following graph shows the field patterns for some of these.





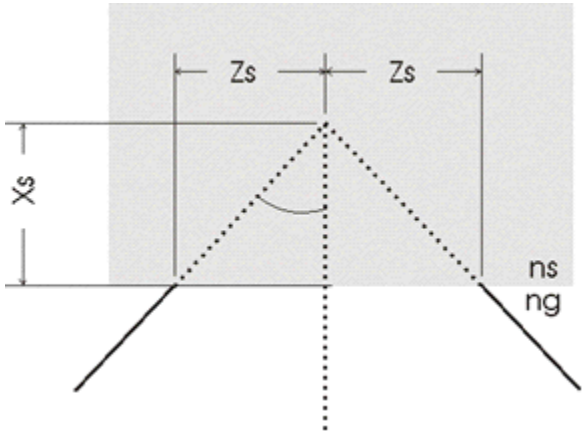
Now it can also be seen that there are other solutions where β takes values other than those for a guided wave. These are described in [34] and the diagram is included below.



There are also other solution as described in [36] that allow for leaky modes that that are guided but diverge at infinity. A description will not be given here but it should be noted when designing a system. This section has given a quick overview of the EM theory of slab waveguides. The ideas outlined here can be extended to a 2-d confined wave in a guiding layer.

6.1.3. Goos-Hanchen Shift

The Goos-Hanchen shift neatly brings together the ray-optic and EM models. The ray optic model first described here assumed that reflections from the substrate and cladding media were R=1. The EM model showed that the solution of the guided light involved some penetration outside the guiding layer where the solution exponentially decayed. The diagram below shows the modified ray optic diagram.



This shows the Goos-Hanchen shift. By trigonometry this can be shown to be

$$S_{GH} = \frac{2N}{k_0\sqrt{N^2 - n_c^2}\sqrt{n_g^2 - N^2}}$$

6.1.4. Modelling

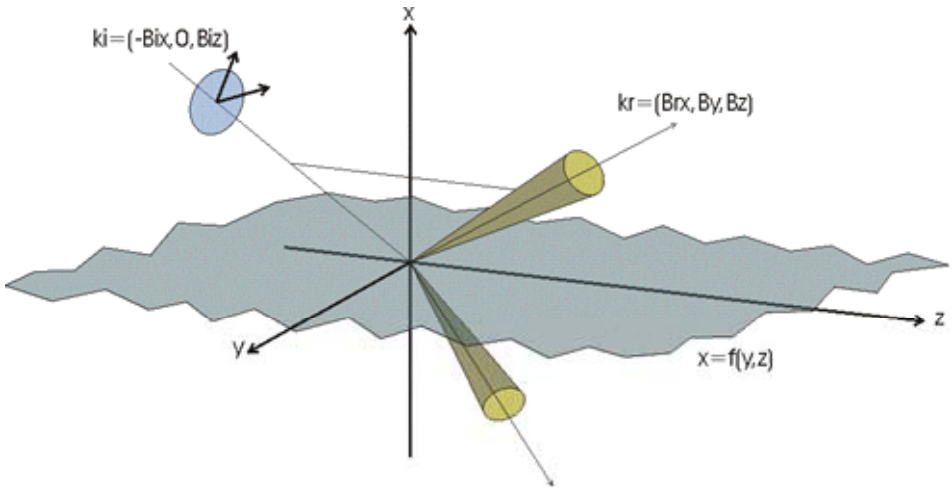
[41] provides modelling packages for waveguides using the beam propagation model and the finite difference time domain model. The former yields fast results but as it approximates the wave equation it has some difficulty modelling high refractive index contrasts and large bends. The latter is more accurate but can take a very long time to model even a short volume of waveguide.
Very simple approximations can be used without resorting to these techniques to sanity check designs. These include the effective index approximation and the method of field shadows. These are discussed in [32].

6.2. Highly Multi-Modal Waveguides Theory and Modelling

Single mode waveguides allow several different structures to be fabricated such as couplers, mux elements etc. but it these are not needed then a larger, highly multi modal waveguide can be fabricated. This has the advantages of easier fabrication and higher tolerance to misalignment of launched light at the expense of higher coupling loss.

For highly multi-modal waveguides, ray tracing is a more relevant theory to use rather than using EM. This is computationally easier and is used in modelling packages such as CodeV [42]. However when applying to polymer waveguides the surface roughness must be taken into account.

[36], [37], [38] give accounts of a method of taking into account the surface roughness of polymer waveguides and a summary is presented here.



If the incident light is given by:

$$E_i^{(s,p)} = E_0^{(s,p)} \cdot e_{s,p} \cdot e^{-j\beta_1 r}$$

where $e_{s,p}$ is a unit vector describing the direction of E_i, β_1 is the wave vector of the incident plane wave, r is the location vector and s and p represent a polarisation dependence then the reflected and transmitted parts can be given by

$$E_r^{(s,p)} = E_0^{(s,p)} \iint g_r^{(s,p)} \cdot e^{-j\beta_r} d\beta_y d\beta_z$$

$$E_t^{(s,p)} = E_0^{(s,p)} \iint g_t^{(s,p)} \cdot e^{-j\beta_t} d\beta_y d\beta_z$$

The parameter g was analytically found to be dependent on the Fourier Transform of the surface roughness ie. the amplitudes of the scattered wave planes are dependent on the Fourier transform of the rough surface.

The rough surface can be described by the function

$$R(u_y, u_z) \approx B \cdot e^{-\left(\left|\frac{u_y}{D_y}\right| + \left|\frac{u_z}{D_z}\right|\right)}$$

Where B is the variance of the roughness and Dy and Dz are correlation lengths.
By using all of the above, the reflected and transmitted waves can then be calculated. By using a Monte-Carlo method where each reflection and transmission yields only one lightpath a calculation can be created to generate the loss due to surface roughness greatly speeded up.

7. Structures

Several common structures are described below.

7.1. Bends

When light is propagated round a bend the mode does not propagate through the centre of the guide but slightly off centre losing energy to radiation. For a single mode waveguide this loss is shown in [32] to be

$$\alpha_{curve} = C_1 e^{-C_2 R}$$

where

R is the radius of curvature and

$$C_1 = \frac{\cos^2\left(k_{xg}\omega\right)\lambda_o e^{2k_{xL}w}}{4k_{xl}n_L\omega^2\left[\omega + \frac{1}{2k_{xg}}\sin\left(2k_{xg}\right) + \frac{1}{k_{xL}}\cos^2\left(\omega k_{xg}\right)\right]}$$

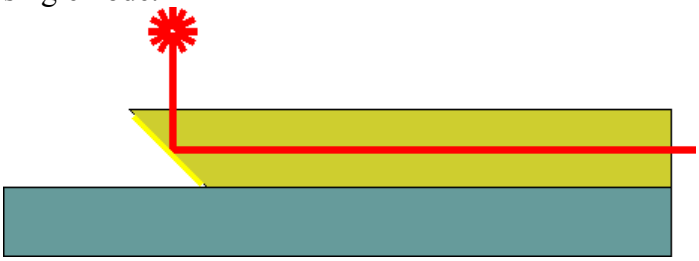
$$C_2 = 2k_{xL}\left(\frac{\lambda_o\beta}{2\pi n_L} - 1\right)$$

where

k_{xg} is the propagation constant pointing tangentially out from the bend, k_{xL} is the decay constant outside the waveguide. The waveguide has width 2ω and β is the propagation constant along the waveguide.

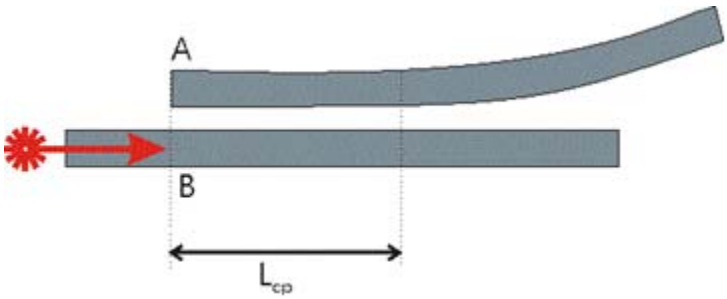
7.2. 90^0 Bends

These structures are only available through laser machining and allow light to be inserted / launched in a surface normal direction. They have been used by [43]. The reflecting surface can be created by total internal reflection but this can be improved by metallisation or thin film coating. The waveguide can be multimode or singlemode.



7.3. Coupler

The diagram below shows the arrangement for a single mode optical coupler.



The evanescent field from waveguide B excites a mode in waveguide A. How much power is transferred is dependent on the proximity and length of the coupling region.

$$(A,B) = (A_0(x,y), B_o(x,y) \cdot e^{j\beta z} e^{j\omega t}$$

$$\frac{dA_o}{dz} = \kappa B_o$$

$$\frac{dB_o}{dz} = -\kappa A_o$$

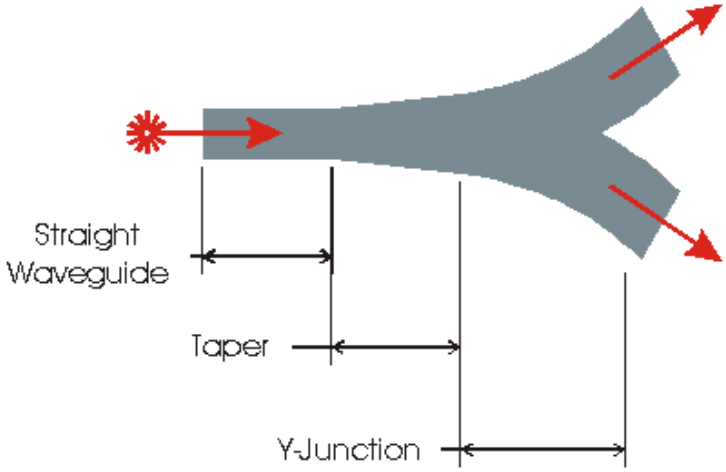
$$A_o(t) = C\sin(\kappa z)$$

$$B_o(t) = C\cos(\kappa z)$$

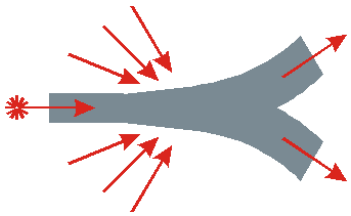
$$\kappa = \frac{2k_{xg}^2 k_{xL} e^{-k_{xl}s}}{2\beta\omega(k_{xL}^2 + k_{xg}^2)}$$

7.4. Y-Junction

A y-junction is shown below.

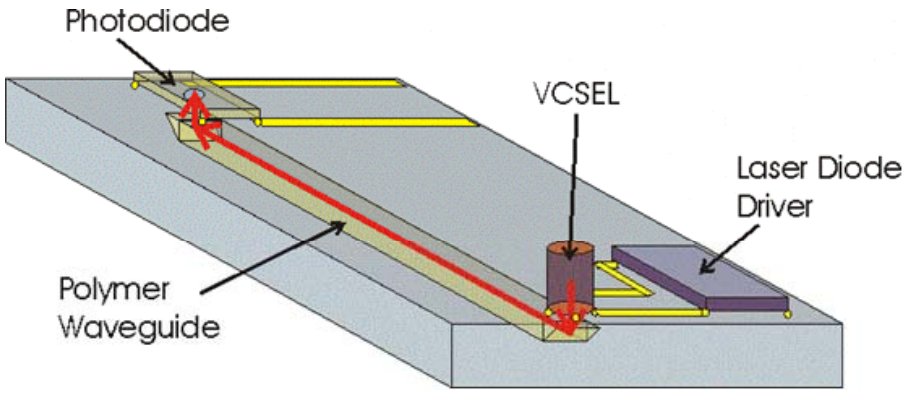


A mode is shown here entering from the left and is split into 2 with portions entering the 2 arms on the right. Depending on the angles of the waveguides any split ratio can be created. However it should be realised that if stray light is allowed to enter the taper before the y-junction the split ratio could be different from intention. The stray light could be from many sources including the weakly guided but divergent light described in the last chapter. This is the worst case as the light could then also be coherent with the light in the waveguide.



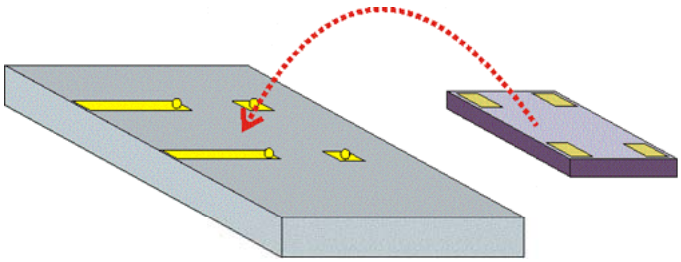
8. Hybridisation

There is not one material that fulfils all the requirements needed for an optoelectronic circuit. The process of packaging together the best devices using various substrates is known as hybridisation. This can be used to create multi chip modules MCM's. The diagram below shows what could be achieved using a PCB substrate with polymer waveguides.



There are various techniques for hybridisation but this chapter will focus on flip chip technologies [51] and the solder techniques associated.

8.1. Flip Chip and Solder Overview



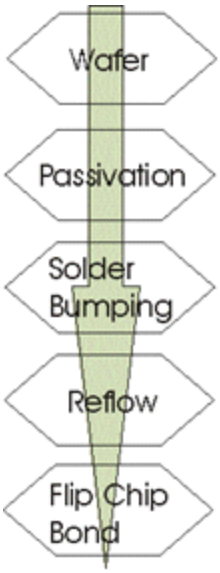
Solder bump flip chip was developed by IBM in 1960. The technology was developed because it was realised that compared to the traditional wire bonding techniques it would yield

- shortest possible leads
- low inductance
- low capacitance
- high frequency
- good noise control
- high density placement
- large number of I/O's
- small device footprints
- low profile

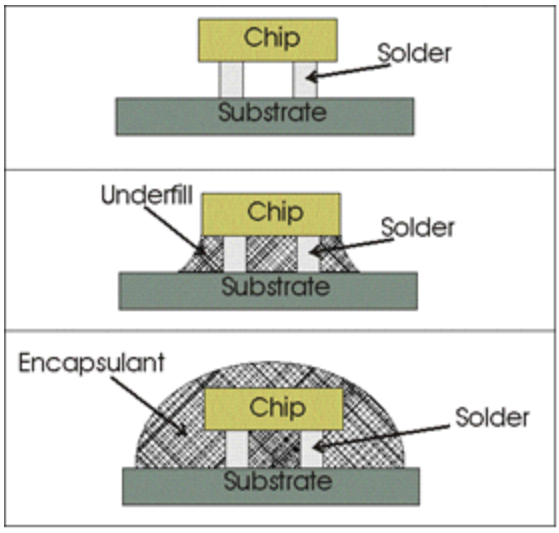
The connections themselves would also have the advantage of serving as a thermal path. It has also been found that using flip chip technology can give lower cost and more rugged design. The table below [52] gives some figures comparing flip chip to conventional wire bonding techniques.

	Worst Case		Best Case	
	Wire Bond	Flip Chip	Wire Bond	Flip Chip
Inductance	19.6 nH	7.9 nH	5.6 nH	0.3 nH
Capacitance	15.0 pF	6.2 pF	9.1 pF	2.5 pF
Resistance	21	2.1	20.1	1.7
Propagation Delay	946 psec	243 psec	508 psec	51 psec

The process flow for flip chipping a chip to substrate is as follows.



Only the last 3 processes will be considered. The actual finished structure can take the forms shown below.



The underfill / encapsulant is to improve reliability by reducing stress.
The processes of flip chip will now be considered.

8.2. Solder Bumping

This section will introduce the under bump metalisation, common solder currently in use and some techniques for fabricating solder.

8.2.1. Under bump metalisation

[42] This layer provides the interface between the substrate and the solder. Common substrates include alumina, glass and silicon.
The layer closest to the substrate is typically Cr, TiW or Ti and provides adhesion between the substrate and the solderable surface. A solderable surface is then layed down eg Cu or Au with a protective layer on top of this eg Au. All of the above is compatible with most metals including Au/Sn. TiPt / Au has been used as a standard with In [45]. [44] gives a list of some under bump metalisation schemes.

8.2.2. Solder Materials

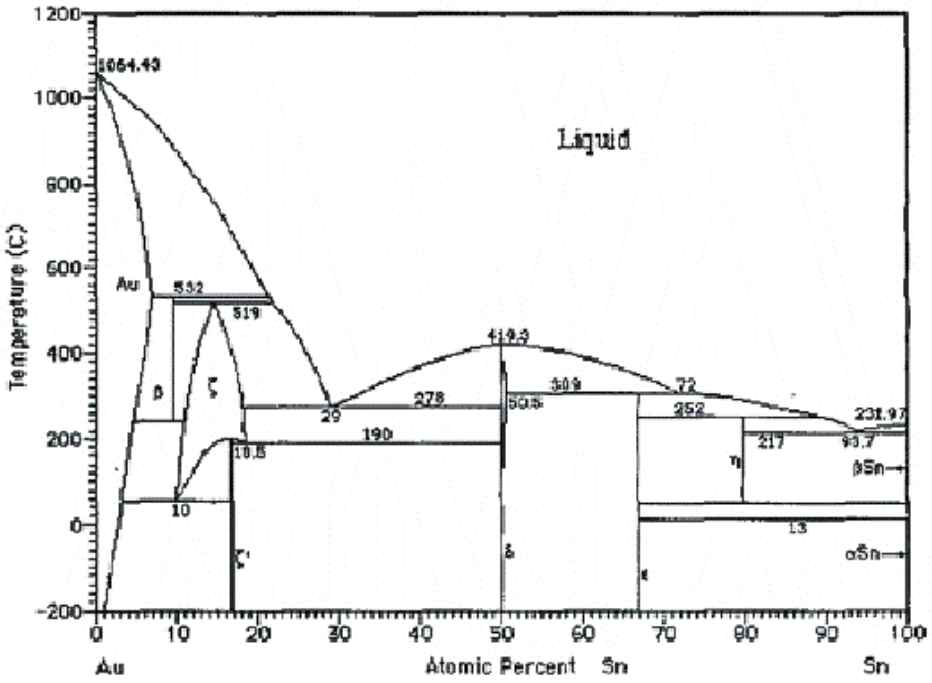
[44] Below is a list of some solders that have been used for optoelectronic hybridisation and some of their properties. A eutectic bond is formed in 2 of the cases. This is a solder in which the alloy formed has a lower melting point than either of the 2 materials on their own. This is only achieved for a certain ratio.

Solder Alloy	Melt T (^{o}C)	E	α	γ	Relative Fatigue Life	Relative creep rate
63Sn37Pb Eutectic	183	30	21	0.4	10	2
90Pb10Sn	268	20	29	0.4	1	1
95Pb5Sn	310	24	26	0.37	1	0.5
80Au20Sn Eutectic	281	68	14	0.4	Poor	N/A
50In50Pb	180		27		3	0.5
100In	157	7	31	0.46	20	Soft
97Sn3Cu	227	41	19	0.33	5	0.01

E: Youngs Modulus (Gpa)
α: CTE (ppm/ ^{o}C) coefficient of thermal expansion
γ: Poisson ratio

It should also be noted that:

- Au/Sn – has no creep but is brittle. Also a fluxless technology. Solder of choice for optoelectronics. The phase diagram is given below



- Indium - good for prototyping but is high cost, large creep rate, poor corrosion resistance, high thermo migration rate and efficient dopant
- Pb/Sn – Used widely in electronics but will be phased out ~2005. Creep rate may give um level misalignment. Pb diffuses into III/V's so should not be used. Cannot be used with gold under bump metallisation as Sn would then try to form 2 eutectic bonds.

- Sn/Cu – creep rate 100 times less than Pb/Sn. Used in automotive industry for lead free solder

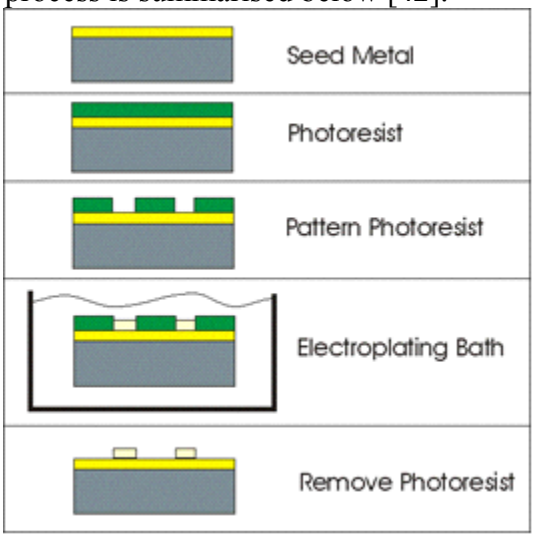
Au/Sn is used the most for optoelectronic attach. The primary reason is that there is no creep, giving a stable alignment over time. It is also favoured as it is a flux free solder.

8.2.3. Solder Technology

This section will explain the process of fabricating solder bumps onto the under bump metalisation. Electroplating, electroless plating, printing, evaporation, micropressing and studbumping will be considered.

Electroplating

The electroplating process is summarised below [42].



The under bump metalistaion or seed metal is placed first. Photoresist is spun on and then patterned. The solder bumps can then be created by repeatedly placing the patterened wafer in electroplating baths to lay down metal. The photoresist is then removed leaving the solder bumps on the substrate. Au/Sn eutectic has been plated onto a TiW/Au layer on a substrate [42], [47] and to Pd/Ag [47]. It should be noted that during reflow the Au/Sn solder composition can be upset as metal is consumed from the under bump metalisation [47], [48], [57]. This can prevented by control of solder composition and composition of under bump metalisation. With electroplating particular care must be taken with current density across wafer. This can effect solder composition, shape and height. It is normal for the Au to be plated first with Sn on top. Although oxidation can occur at the Sn air boundary this is not thought to be a problem

Electroless

[42]Electroless plating has the highest potential for cost reduction. Electroless metal plating is a proven technology and is a standard process for corrosion protection of aluminium. In this instance aluminium is coated with nickel. However electroless solder plating is still in developmemt. It is a cheap process as there is no sputtering, photoresist imaging or electroplating. The plating mechanism is by autocatalytic metal deposition. For this to work it only requires contact between electoless plating solution and wafers. An Al pad must be used as the first layer. However Al readily forms oxide so a thin layer of zincate is deposited. Before this deposition the Al is cleaned first by wet or dry etch.The zincate is then deposited by immersion with the process shown below.

$$Al^0 + 3OH^- = Al(OH)_3 + 3e^-$$
$$Zn(OH)_4^{-2} = Zn^{2+} + 4OH^-$$
$$Zn^{2+} + 2e^- = Zn^0$$

Electroless nickel can then be deposited on top of this. Pure nickel does not support electroless deposition so either nickel phosphorous or nickel boron is used. The reducing agent in these cases is hypophosphorous acid and DMBA respectively. During the reaction of the reducing agent, phosphorous or boron is produced. Therefore the metal layer produced is not pure metal but is NiP and NiB alloys. NiP can be deposited at a rate of 25um/hour. Although not solder this can be applied to seal in an Al pad to prevent oxidation.
Solder deposition is not an autocatalytic process, howevere IZM [58] have developed an electroless processes for PbSn and AuSn.
Note that for electroless deposition lateral and vertical growth are approximately the same leading to a mushroom shaped pad. 50um pitch is an achievable pitch between pads.

Printing

Printing of solder bumps is a cheap process [42]. The process is as follows. Paste is pushed into holes on a stencil covering the substrate. The stencil is retracted and the bump prebaked. It is then ready for use.

Evaporation

Evaporated formation gives the best uniformity in composition and volume. The minimum size and pitch determined by metal mask technology [42]. However the evaporation machinery does make this a slow and expensive process [25].

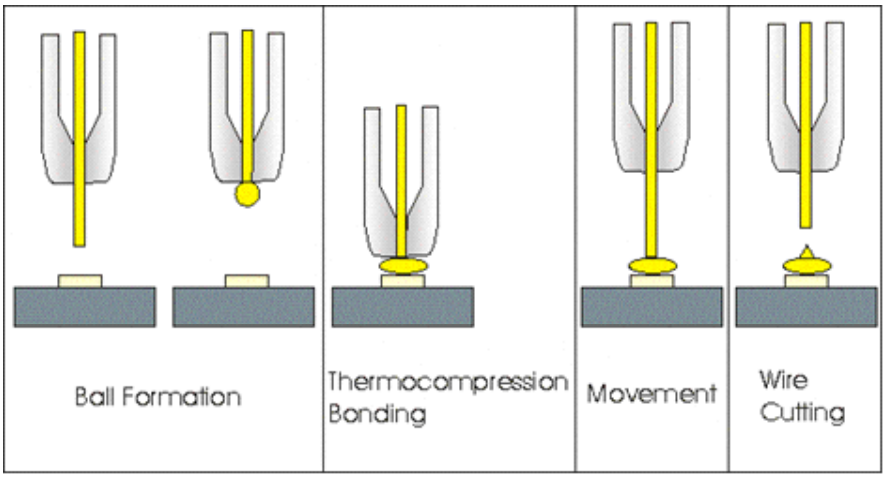
Micro Press

The micro-press technique has been discussed by [43]. A ribbon of Au / Sn is created and passed over the substrate to be bumped. A punch comes down and presses a bump

onto the substrate. This is then reflowed so that it wets onto the solderable area. Bumps of 100um diameter have been created using this technique

Stud Bumps

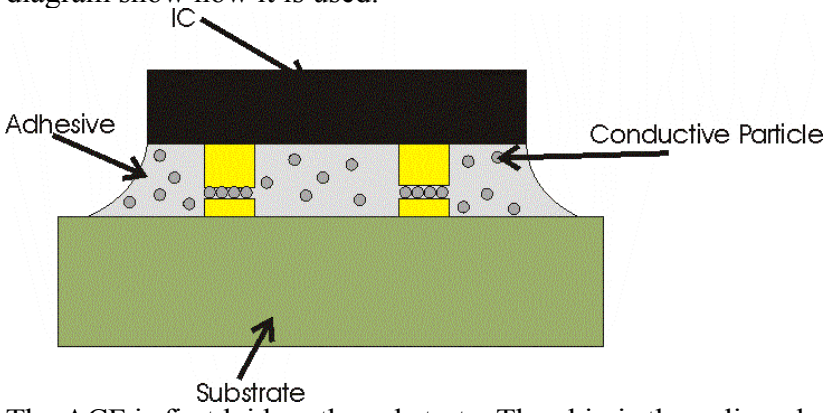
Stud bumps are a metal rather than a solder contact and can give the best electrical contact. They do however require more force and temperature to form the bond. The diagram below shows the steps needed to form a stud bump [42].



Gold wire passed through through the capillary tube of the wire bond machine. There is then an electrical discharge to form gold ball. The gold ball is then bonded to the pad by thermocompression. Ultrasonic energy can also be used at this stage. The capillary is then withdrawn and the wire cut leaving the metal pad on the substrate ready for bonding. It should be noted that the Youngs modulus of the bonding wire must be high to form uniform height. It is for this reason that gold is preferred. Although there are references in the literature to stud bumping [42], [55], [56] there are no figures detailing the forces and temperatures needed. It should be noted that bump diameters of 50um have been achieved. Discussion with Changhai Wang at HWU has suggested that Au stud bumping with thermocompression would need forces ~100g per pad.
[53], [54] report on stud bumping of the under bump metalisation. This however requires a non-standard solder.

ACF

ACF is anisotropic conductive film technology. This has also been called z-axis conductive adhesive. It is designed to be conductive in the z direction ie between chip and substrate and insulating in the horizontal direction ensuring no short circuits. The adhesive left under the chip acts as underfill. It should be noted that applications have only been found where there is no active area on the adhesive side. The following diagram show how it is used.



The ACF is first laid on the substrate. The chip is then aligned and the adhesive cured. A good contact assumes that the density and distribution of the conducting particles is such that when the IC and substrate are in contact it is assured that there will be enough particles between the pads. One shortcoming of this method is that the amount of particles between the pads cannot be controlled implying the possibility of some poor electrical contacts.

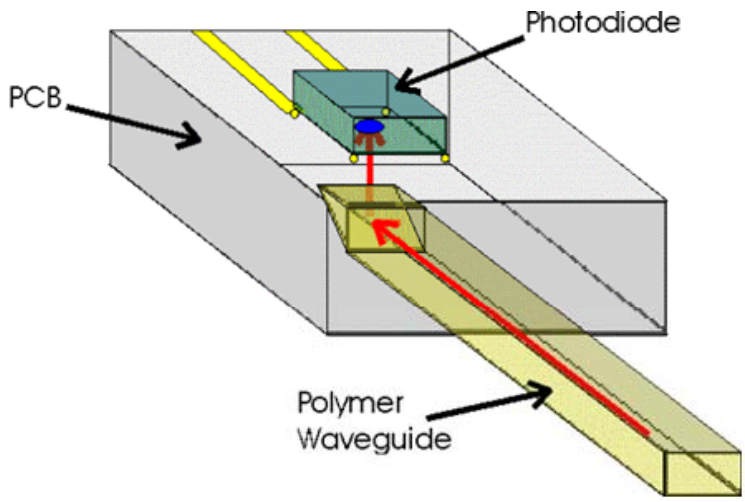
8.3. Alignment and Attach

When active devices are attached there are several ways of ensuring that they are aligned to the waveguide as required. This is a critical parameter for single mode waveguides and is typically in the sub-micron range. For multimode waveguides several microns could be tolerated. This section will discuss each technique of alignment and attach in turn.

8.3.1. Machine Alignment

[52] This technique relies on the accuracy of the machine that will align and bond. There are many ways of ensuring accuracy but all rely on the alignment of marks called fiducials on the chip and substrate. Whatever material is used to form these marks they should have good contrast with the substrates. The chip is then brought into contact with the substrate and the solder reflowed by ramping the temperature in the substrate and /or the chip. Some force may be applied as this occurs.

8.3.2. Active Alignment



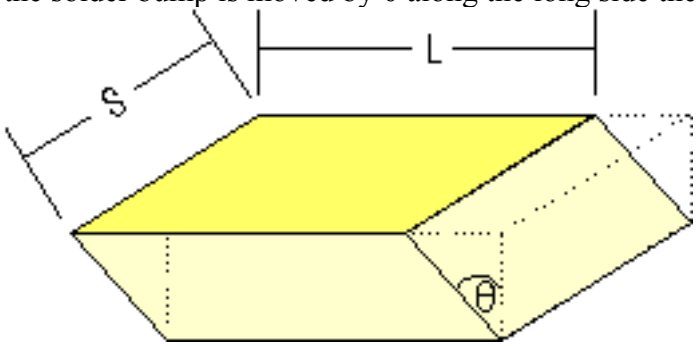
This is best explained by example. To align the PD, light would be launched into the waveguide and the PD moved into such a position that the photocurrent is maximised. This method is time consuming and requires dedicated machinery.

8.3.3. Self Alignment

A general rule is that if the chip is misaligned to the intended position by less than 25% of the bond pad dimension the reflow process is capable of self alignment [42]. This means that the chip can be tacked with less accurate machinery and then reflowed to perfect alignment. This would also allow multiple attaches to be carried out.

[46] reports on self alignment of a laser to a waveguide using a rectangular pad. It states that it is important for the lateral alignment to occur first, followed by a slow axial alignment. The reasoning is that if the laser moves in the axial direction first it will be in contact with the waveguide which will exert a frictional force. This will work against the self alignment mechansim.

If S and L are the length of the short and long side and H is the bond height, then if the solder bump is moved by θ along the long side the change in the surface area is:



$$\Delta A_L = 2S\left(H/\cos\theta\right) - 2SH$$

$$= 2SH\left(1/\cos\theta - 1\right)$$

and if the pad is moved along the short side the change in surface area is:

$$\Delta A_S = 2L\left(H/\cos\theta\right) - 2LH$$

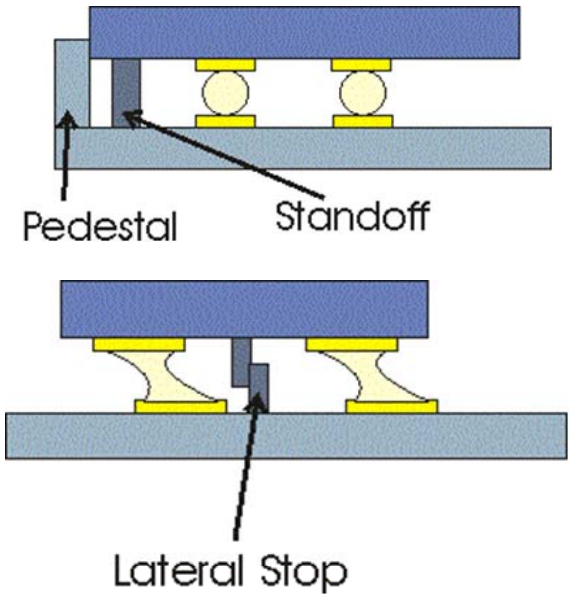
$$= 2LH\left(1/\cos\theta - 1\right)$$

As L > S then ΔA_s is larger than ΔA_L hence the restoring force is greater along the short side. Using this geometry the lateral alignement occurs first.

[43] also reports on self alignment using similar stripe bumps.

8.3.4. Self Alignmnet with Stops

[44] Builds on the idea of self alignment by introducing stops. This relies on structures built into the substrate in such a way that when the restoring force of the solder at reflow is applied the chip will stop in the position specified by the structures. This is shown in the diagrams below. This adds another level of complexity to the solder design, but could yield very accurate results.



8.4. Underfill – Encapsulate

Underfill and encapsulation are important as they improve reliability by reducing thermal stresses around chip. The cure time and temperature of the fill material must be chosen so that the solder does not reflow. A 25um gap is usually needed to ensure the fill material can flow under the structure. Flow under the chip can be improved by adding trenches that extend from under the chip.

8.5. Considerations

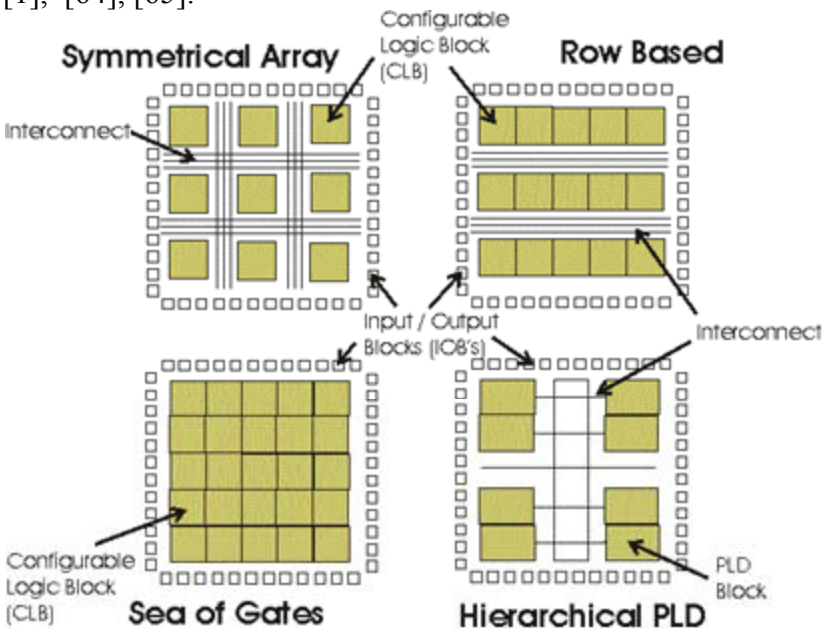
There are some overall considerations when designing for a flip chip solder bumped interface. The solder characteristics of creep, maximum reflow temperature and resistance should be compatible with the other processes and requirements of the system. If there are to be multiple attaches the bonding process should either be compatible with multiple reflows or the bonding sites should be sufficient distance apart that other parts will not reflow. The overall stresses seen by the chip over the working temperature range of the system should also be looked with attention paid to thermal expansion mismatch.

9. FPGA: An Example

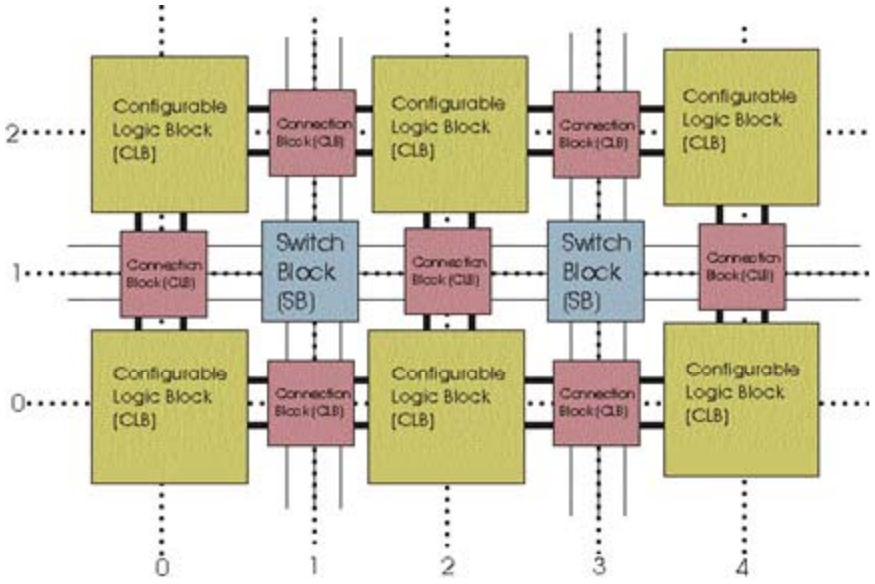
This section should bring together some of the ideas presented in the preceding chapters.

9.1. FPGA Basics

An FPGA is a field programmable gate array. The diagram below shows the layout of such chips [1], [64], [65].



An FPGA consists of logic blocks with interconnections in between. As shown in the next diagram there are switching blocks and connection blocks on these interconnections.



The switching blocks and connection blocks are user definable, meaning that the chip can be reconfigured as to what its functionality is. This gives the FPGA is usefulness [63].
The flexibility is at the expense of chip real estate taken up by interconnections Some 70% of the chip can be taken up by interconnects. As stated in Chapter 2 the global connections on a chip run at a slower speed than local connections. This amount of interconnection can create some problems as illustrated in the following example.

9.2. Multiple FPGA's

[59], [61], [61], ASIC's are a static chip deisgn for a particular purpose but havs the disadvantage of long design times. FPGA's being off the shelf parts are available immediatley are cheaper and can be reconfigured to emulate an ASIC. However due to the amount of interconnection there is less room for logical elements. Therfore to replicate some ASIC designs, multiple FPGA's will have to be interconnected together. This means that unlike the ASIC components on chip there will be signals traversing the electronic interconnects across PCB and potentially across multiple FPGA's.
This bottleneck could be alleviated by using optical interconnection.
Lasers and photodiodes could be hybridised onto the middle of a FPGA with the light surface normal. A network of chips could then be connected by waveguides with 90deg mirrors. The interconnects across PCB are then eliminated and replaced with a high speed interconnect and the longest interconnect length across the FPGA reduced. By intelligent selection of the network needed for the application a fast alternative to an ASIC would be realised.

10. Conclusions

This purpose of this literature survey was to give an overview of electronic interconnect patterns, polymer waveguides and FPGA's. Each of these ideas was taken in turn and an overview of the theory, fabrication and application briefly explained.

Current electronic interconnects will be limited in speed both at chip and board level in the near future. Optical interconnection and specifically polymer waveguides have been posited as a possible alternative. The actual mechanism of implementing polymer waveguides on PCB's was examined and different aspects of hybridising active elements to the PCB discussed. The concept of an FPGA was finally given and an application using FPGA's presented that used some of the concepts given in the preceeding chapters.

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